

iCD Design Integrity

incorporates the iCD Stackup and PDN Planner software. Offers PCB Designers unprecedented simulation speed, ease of use & accuracy at an affordable price

Dielectric Materials Library
30,700 Rigid & Flex Materials to 100GHz

Termination Planner
Extracts IV Curves from IBIS Models
Calculates Series Terminator of the Distributed System Including Loads

iCD Stackup Planner - Offers Engineers & PCB Designers unprecedented simulation speed, ease of use and accuracy at an affordable price

- Industry Leading 2D (BEM) Field Solver precision
- Characteristic impedance, edge-coupled & broadside-coupled differential impedance
- Relative Signal Propagation with 'Matched Delay Optimization'—ideal for DDRx design
- Termination Planner - series termination based on IBIS models & distributed system
- Unique Field Solver computation of multiple differential technologies per signal layer
- Extensive Dielectric Materials Library –over 30,700 rigid & flexible materials up to 100GHz
- Interfaces—Allegro, Altium, Excel, HyperLynx, OrCAD, PADS, Zmetrix TDR, Zuken & PC-2581B

iCD PDN Planner - Analyze multiple power supplies to maintain low AC impedance over entire frequency range dramatically improving product performance

- Fast AC impedance analysis with plane resonance and projected EMI
- Definition of plane size, dielectric constant & plane separation
- Extraction of plane data from the integrated iCD Stackup Planner
- Definition of voltage regulator, bypass/decoupling capacitors, mounting loop inductance
- PDEMI Plot with FCC, CISPR & VCCI Limits. Frequency range up to 100GHz
- Extensive Capacitor Library –over 5,650 capacitors derived from SPICE models

“iCD Design Integrity software features a myriad of functionality specifically developed for high-speed design.”
- Barry Olney



Ground Bounce

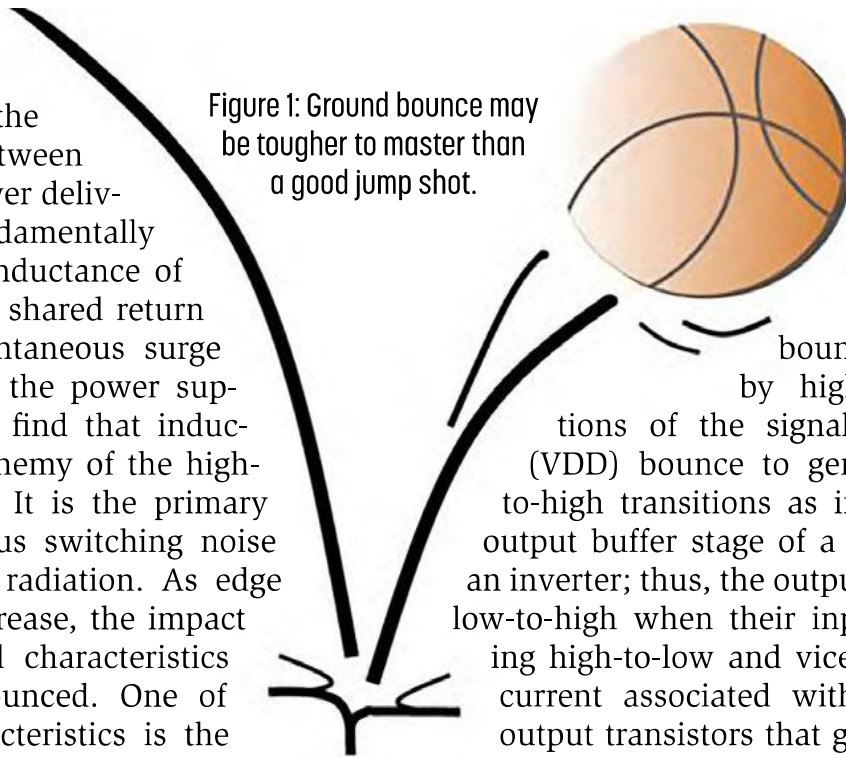
Beyond Design

by Barry Olney, IN-CIRCUIT DESIGN PTY LTD / AUSTRALIA

Ground bounce, or more precisely, supply bounce, is the voltage produced between two points in the power delivery path. It is fundamentally related to the total inductance of the current path and shared return paths and the instantaneous surge current delivered by the power supply. Once again, we find that inductance is the covert enemy of the high-speed PCB designer. It is the primary cause of simultaneous switching noise and electromagnetic radiation. As edge rates continue to increase, the impact of intrinsic electrical characteristics become more pronounced. One of these inherent characteristics is the inductance found in the supply leads of all ICs. In this month's column, I will look at supply bounce and how to minimise the impact on high-speed digital circuits.

Ground bounce arises from a common-mode potential developed between an IC die substrate and the PCB ground return plane and is totally independent of the transmission line characteristics. The physical location of the device driver within the IC as well as the number of outputs that are simultaneously switched, with respect to the common power and ground connections to the die, also has an impact. In addition, ground bounce is associated with the di/dt (change

Figure 1: Ground bounce may be tougher to master than a good jump shot.



in current over time) of the output which depends on the switching speed of the driver gate.

Ground (GND) bounce is generated by high-to-low transitions of the signal, whilst power (VDD) bounce is generated by low-to-high transitions as in Figure 2. The output buffer stage of a CMOS device is an inverter; thus, the outputs are switching low-to-high when their inputs are switching high-to-low and vice versa. It is the current associated with switching the output transistors that generates ground bounce. Note that everything discussed here concerning ground bounce can equally be applied to the opposite effect: VDD bounce.

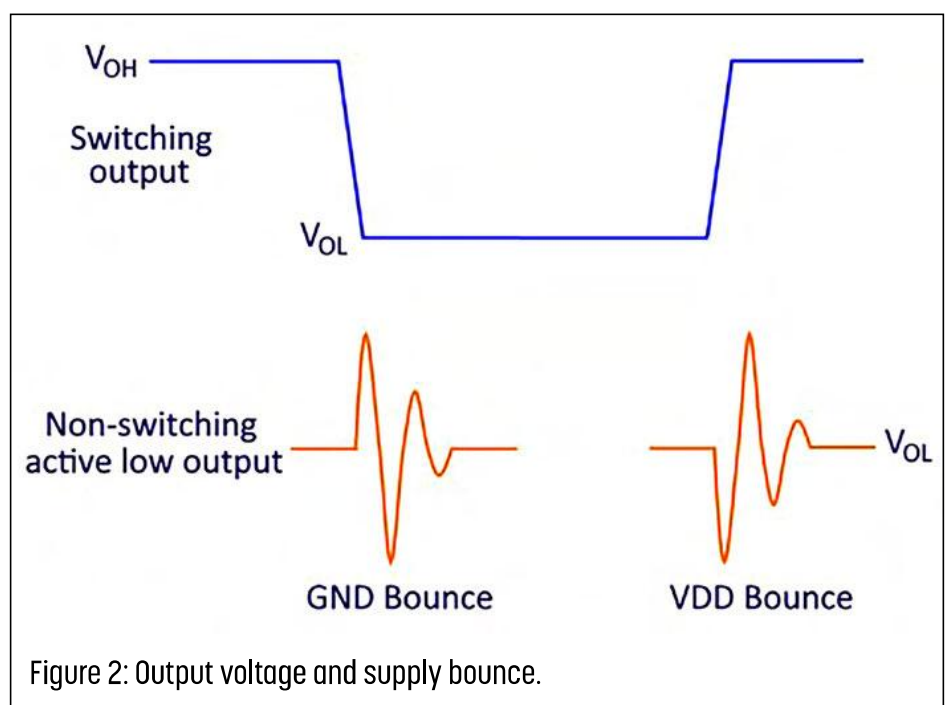


Figure 2: Output voltage and supply bounce.

When supply bounce occurs, the charge that is impressed across the power delivery path results in common-mode voltage. Unfortunately, it is not possible to eliminate the transfer of charge between logic transitions but the magnitude of the radiated peaks can be limited by providing a very low AC impedance path between power and ground. This is why power distribution network (PDN) planning is so important. The AC impedance of the power planes must be maintained below the target impedance up to the maximum bandwidth.

The measured supply bounce is generally very small (typically 150mV) compared to the full rail voltage swing of the output signal. So, its presence does not impact on the transmitted signal. However, it does interfere with the reception of the signal at the load, depending on the noise margin, and can cause double clocking. This is because a TTL receiver compares the input voltage against the local 0V ground reference plane. CMOS devices compare the input voltage to the weighted aver-

age of the VDD and GND while ECL compares it to VDD. Although the topology is different between logic families, the concept of supply bounce is the same. If N outputs are simultaneously switched, then there is N times as much current and therefore the supply bounce pulse is N times larger.

Figure 3 depicts the simplistic view of how supply bounce is generated. When the input to the driver transistor (right) goes high, the output goes low (V_{OL}), and a surge of current is pulled through the output ball of the BGA package from the capacitive load. This current flows through inductor L_{GND} , representing the matrix of ground balls beneath the BGA package, causing a voltage glitch on the IC die substrate. There are typically multiple GND and VDD pads, on the BGA package, so that the parallel combination reduces the overall inductance of L_{GND} and L_{VDD} , respectively. The victim, non-switching output (left), remains active low. However, the voltage glitch, on the substrate, is coupled into the output, and is transmitted out of the pin.

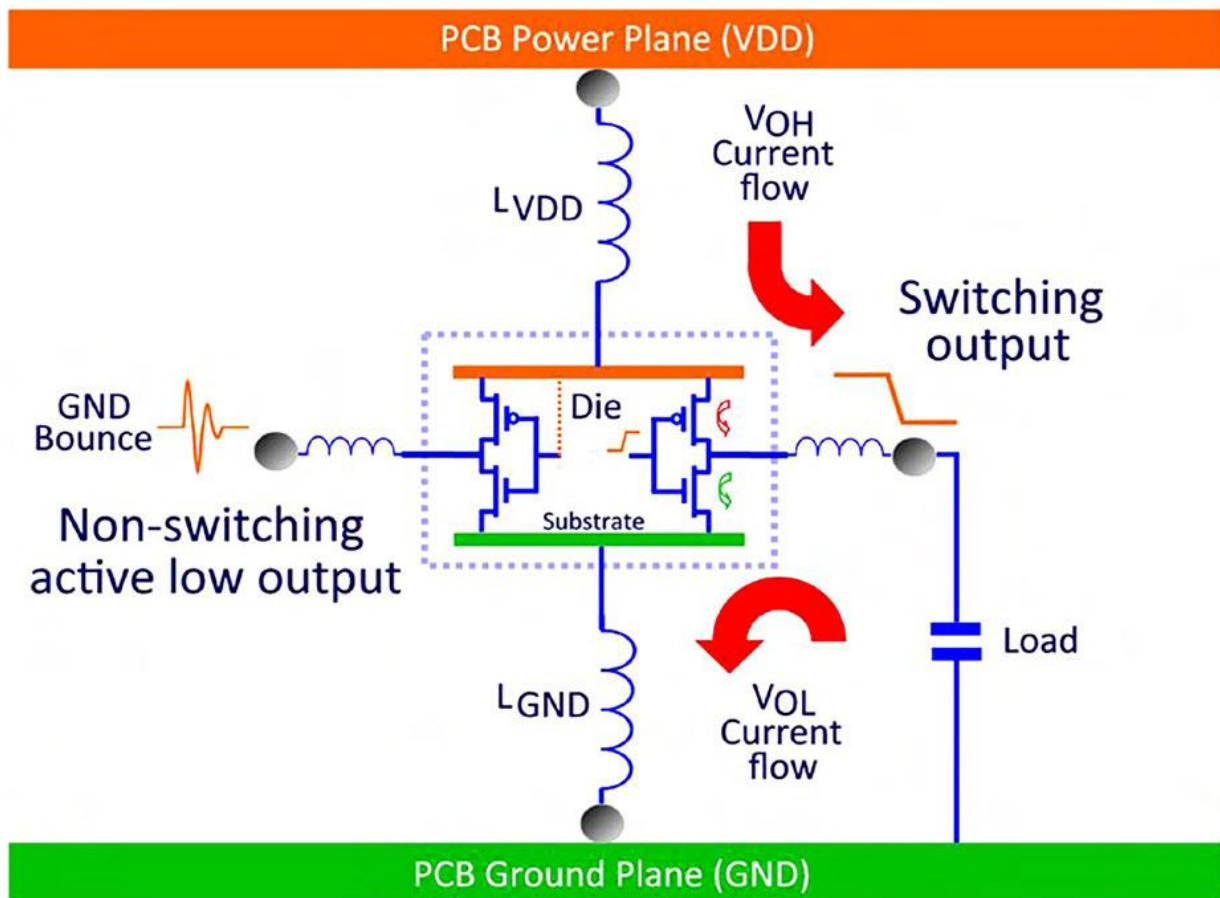


Figure 3: Generation of supply bounce in a BGA package.

There may be hundreds of such outputs on an IC, which all simultaneously impart switching noise onto the planes. The opposite applies to VDD bounce; when the output switch pulls the output voltage high (V_{OH}), the current surges through L_{VDD} to the load.

Supply bounce gets worse as a result of the following conditions due to the increased current drawn from the PDN:

1. Capacitive load increases
2. Load resistance decreases
3. Lead and trace inductance increases
4. Multiple gates switch simultaneously

At high-speeds, the lead inductance of an IC package is critical. Larger packages tend to have more lead inductance. Wire bond, tape automated bonding (TAB) and flip-chip IC packages dramatically reduce the internal inductance by shortening the supply lead connections between the IC die substrate and the PCB planes.

Fortunately for PCB designers, there are a number of approaches that can be implemented, particularly during layout and routing of the PCB, to minimize the voltage drop, hence supply bounce, in the power delivery path:

1. Decrease the rate of change in the loop. Where possible, slow down the edge rates by employing series terminations. Also, some ICs now have clock skew adjustment to slow down the edge rate in addition to on-die terminations which are used to alleviate the need for external terminations.

2. Decrease the total loop inductance of the return path. Make the return path as short and wide as possible.

3. Bring the signal and return path closer together. This increases coupling and ensures that the return path follows the signal with a minimum loop area.

4. Limit the number of signals that share the same return path. A separate ground and VDD connection should be provided for each IC pin, directly connected to the ground or power

plane, during the fanout routing of the package. Connecting two or more pins together, and then routing them through the same trace to a common grounding via, defeats the purpose of multiple ground and power pins.

5. Minimize the inductance of the planes during layout by using wide plane pours rather than thick traces.

6. Use thin (<5mil) dielectric core materials between the power and ground planes. Or better still, use embedded planar capacitance to provide additional low inductance decoupling to the IC.

7. Optimize the power distribution network by analyzing the decoupling requirements across the entire frequency bandwidth. Low AC Impedance reduces radiation.

8. Locate power and ground vias adjacent to each other, where possible, so that the magnetic flux is cancelled which minimizes common-mode currents.

9. Preferably, select IC packages that have a large central grounding pad under the package and connect it using multiple vias to reduce the inductance to ground. Also, select a package that has a high ratio of ground and power pins compared to signal pins. BGAs generally provide this but other SMT packages have limited supply pins.

10. Choose an IC with the lowest drive current output that will provide the required performance. This reduces the amount of current available to rapidly charge the system capacitance, directly reducing ground bounce.

11. Stagger the timing of output pins on a device. Spreading the switching time of many outputs over an extended period can substantially reduce ground bounce at the IC level.

12. Use differential signaling and avoid common-mode currents. Differential-mode is converted to common-mode at any imbalance in the pair. So it is best to correct any disparity as soon as it occurs by adding extra length, hence delay.

Supply bounce cannot be eliminated and problems occur when its combined amplitude becomes excessive. However, low inductance and low AC impedance of the power distribu-

tion network reduce the impact of simultaneous switching noise and electromagnetic radiation in high-speed digital PCB designs.

Key Points

- Supply bounce is fundamentally related to the total inductance of the current path or shared return paths. It is the primary cause of simultaneous switching noise and electromagnetic radiation.
- When supply bounce occurs, the charge that is impressed across the power delivery path results in common-mode voltage. It is this common-mode voltage that creates electromagnetic emissions.
- The magnitude of the radiated peaks can be limited by providing a very low AC impedance path between power and ground.
- Supply bounce interferes with the reception of the signal at the load, depending on the noise margin, and can cause double clocking.
- Supply bounce gets worse as the result of increased lead inductance, capacitive load and simultaneously switching outputs. It also deteriorates with reduced resistive load.

- At high-speeds, the lead inductance of an IC package is critical. Larger packages tend to have more lead inductance.
- A number of approaches can be implemented during layout and routing of the PCB to minimize the voltage drop, hence supply bounce, in the power delivery path.

References

1. Barry Olney's Beyond Design column, [The Dumping Ground](#).
2. Understanding and Minimizing Ground Bounce, Fairchild Semiconductor.
3. [EMC and the Printed Circuit Board](#), Mark Montrose.
4. [Signal and Power Integrity – Simplified](#), Eric Bogatin.
5. [High-Speed Digital Design](#), Howard Johnson.



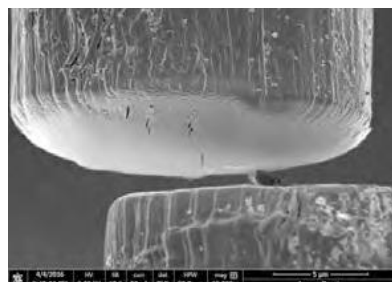
Barry Olney is managing director of In-Circuit Design Pty Ltd (iCD), Australia, a PCB design service bureau that specializes in board-level simulation. The company developed the iCD Design Integrity software incorporating the iCD Stackup, PDN and CPW Planner. The software can be downloaded from www.icd.com.au. To contact Olney, or read past columns, [click here](#).

Nanotube Fibers in a Jiffy

A method developed by the Rice lab of chemist Matteo Pasquali allows researchers to make short lengths of strong, conductive fibers from small samples of bulk nanotubes in about an hour. The work complements Pasquali's pioneering 2013 method to spin full spools of thread-like nanotube fibers for aerospace, automotive, medical and smart-clothing applications. The fibers look like cotton thread but perform like metal wires and carbon fibers.

It can take grams of material and weeks of effort to optimize the process of spinning continuous fibers, but the new method cuts that down to size, even if it does require a bit of hands-on processing.

Pasquali and lead author and



graduate student Robby Headrick reported in *Advanced Materials* that aligning and twisting the hair-like fibers is fairly simple.

First, Headrick makes films. After dissolving a small amount of nanotubes in acid, he places the solution between two glass slides. Moving them quickly past each other applies shear force that prompts the billions of nanotubes within the solution to line up. Once the resulting films are deposited onto the glass, he peels off sections and rolls them up into fibers.

Pasquali said the process reproduces the high nanotube alignment and high packing density typical of fibers produced via spinning, but at a size sufficient for strength and conductivity tests.