# Effective Floor Planning Strategies

**by Barry Olney,** In-Circuit Design PTY LTD / Australia

**Component placement on a** printed circuit board is more involved than simply fitting parts into available space. It plays a pivotal role in determining the board's overall manufacturability, performance, reliability, and cost. Poor placement can compromise even the most meticulously designed PCB. Effective component placement alleviates mechanical stress, promotes efficient thermal management, and helps prevent excessive heat buildup. Conversely, poor placement can lead to soldering obstructions, assembly and inspection challenges, increased layer counts, signal integrity issues, power noise, and electromagnetic compatibility failures.

Anyone who thinks placement is easy has never tackled an RF or high-speed layout. In this month's column, I'll delve into the high-speed considerations that make effective floor planning both an art and a science.

Before we begin placement, establish the layer stack. Stackup planning establishes the foundation, while placement orchestrates the execution. For instance, the iCD Stackup Planner gives you the dielectric precision and impedance clarity to make confident layout decisions. Use the stackup to decide where sensitive nets should live, then place components to ensure clean transitions between those layers. Run impedance targets for the required single-ended and differential pairs, set by the technology used. Based on the

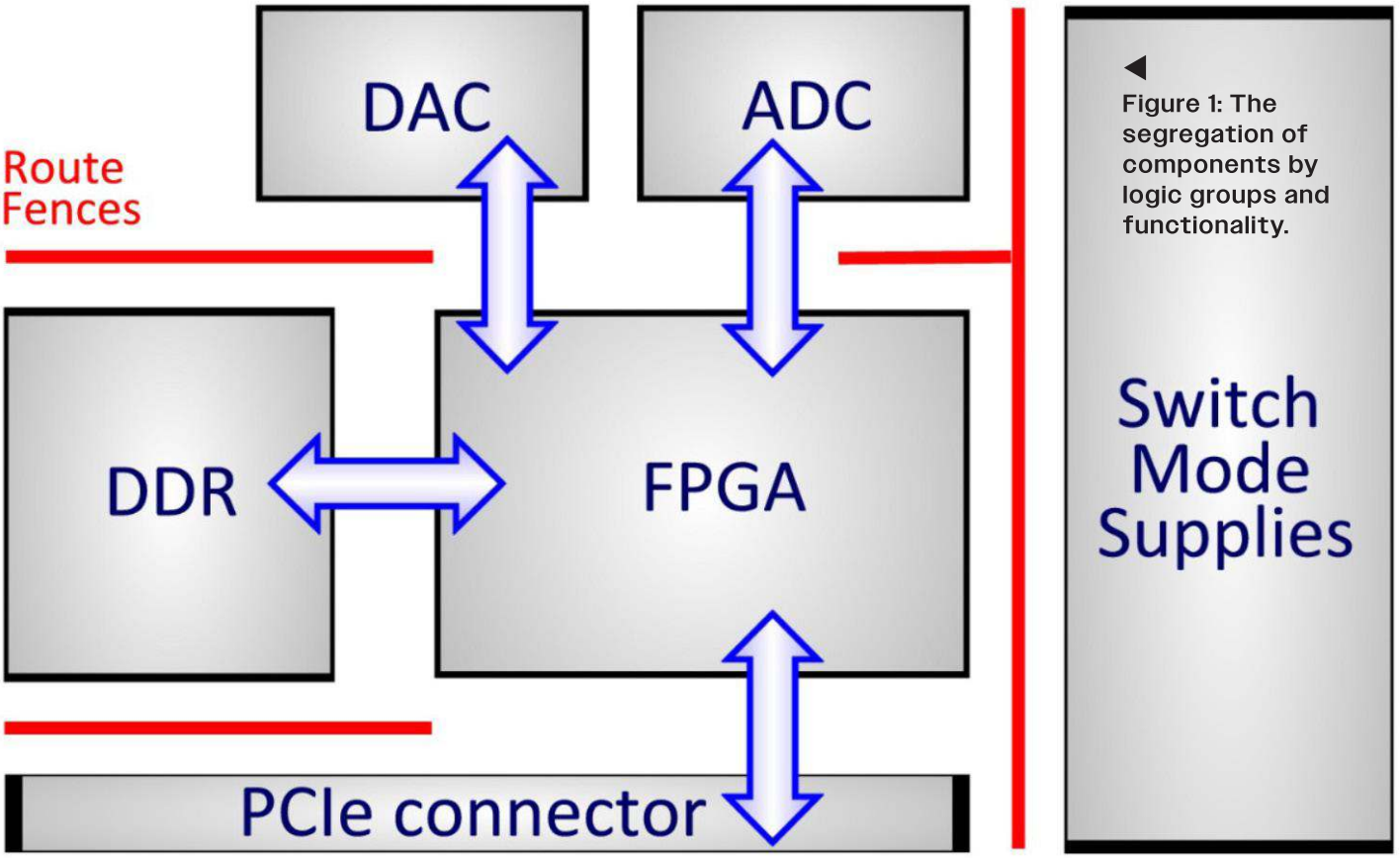
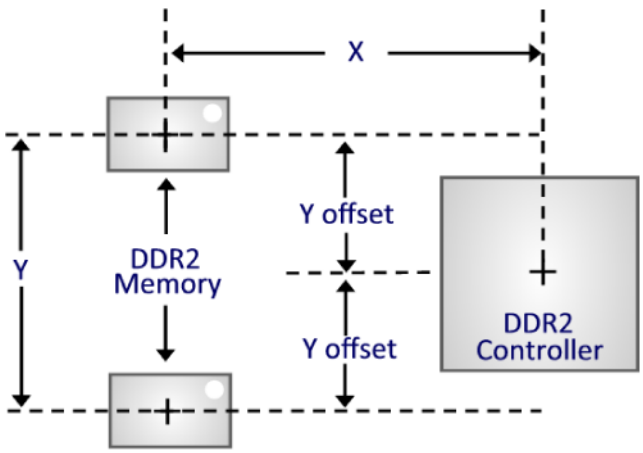
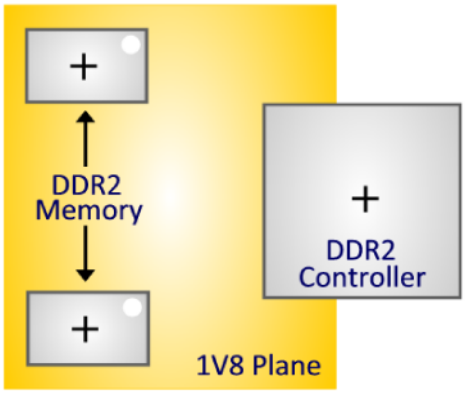



Figure 1: The segregation of components by logic groups and functionality.




◀ Figure 2: Processor and memory device placement requirements with 1.8V plane.

selected materials and spacing, determine the ideal routing layers. Then, place high-speed components (clocks, SerDes, DDR) to minimize trace, stub length, and via count on those preferred layers. Pay particular attention to the flight time and skew of the critical signals.

It is advisable to partition component groups based on rise-time and operating frequency, positioning the highest-speed devices closest to the connector, as illustrated in Figure 1. Subsequent placement should follow a descending order of signal speed, with analog sections located furthest from the connector to reduce the risk of noise coupling into sensitive circuitry. Electrically isolate switch-mode power supplies while maintaining a continuous common ground plane. Special attention should be given to minimizing net crossovers to improve routing efficiency.

It is essential that all analog signals are routed within the analog section, while digital signals are confined to the digital section, both sharing a continuous common ground plane. Control signals may traverse between these domains as needed. Over the years, I've employed a proven method to enforce this segregation: route fences or keep-outs. We implement these by placing elongated keep-out zones across signal layers, effectively guiding the routing process and preventing signals from crossing designated boundaries on specific layers. Figure 1 illustrates a typical application of this technique.

It is important to remember that high-speed return currents follow the path of least inductance. For example, when a trace runs from an analog-to-digital converter (ADC) to an FPGA, the return current will flow directly beneath that trace, avoiding nearby sections. Route fences also help control the autorouter by preventing signals from crossing boundaries while allowing control signals to pass through.

Since crosstalk is caused by an aggressor signal coupling onto a victim signal, higher aggressor voltages induce more crosstalk. To mitigate this, it is advisable to segregate groups of nets based on their signal amplitudes. This prevents higher voltage nets (such as 3.3V) from affecting lower voltage nets (such as 1.5V), which have reduced noise margins.

Signal flight time and skew are critical considerations in high-speed PCB design. A primary factor influencing these parameters is the placement of components. By controlling the placement of devices and assuming adherence to good design practices, the maximum signal delay can be approximated by the longest Manhattan (X + Y) distance within a specific clock domain. Route the clocks/strobes first within a group, without serpentine patterns initially. This allows for accurate skew matching later in the process, as nets with higher signal velocity can be lengthened to align with the longest propagation delay, ensuring synchronized signal arrival across all critical paths.

The clock should always have the longest delay so the data and address lines have time to settle before being clocked. Consequently, flight time and skew for an entire clock domain are determined by the maximum placement and routing rules that enforce trace delay matching. However, there is a sweet spot. If the distance between the

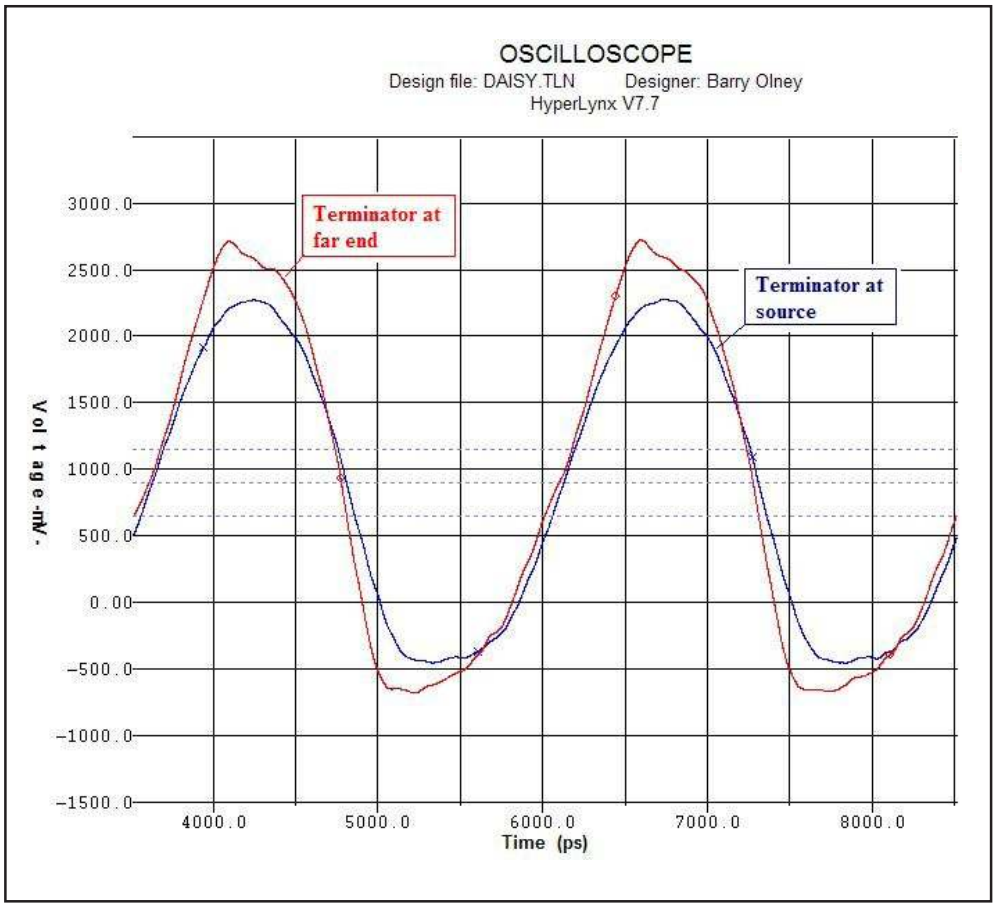
controller and memory is too compact, then trace tuning becomes a challenge; too far, and signal propagation delays increase.

In traditional high-speed design workflows, timing specifications and simulation results guide the establishment of placement and routing constraints. With a given delay constraint, designers can manage signal integrity by controlling the PCB trace topology across different interface components.

Figure 2 illustrates the placement requirements for a DDR2 controller and memory chips, along with the 1.8V power plane. However, this applies to all memory interfaces. The placement guide aims to limit maximum trace delays and facilitate routing and via placement challenges. It is important to note that this placement does not specify whether these devices are positioned on the top or bottom of the board.

The DDR circuitry region must be isolated from other signals to prevent interference while maintaining a common ground plane. A designated keep-out zone, as shown in Figure 2, can achieve this. The 1.8V power plane should encompass this entire region and non-DDR signals should be kept outside of it to maintain signal integrity and proper operation. Also, the placement of series terminators, when required, can present layout challenges. In the absence of a termination at the far end of the trace, the series terminator must be positioned to effectively absorb the full reflection returning from the load.

Figure 3 illustrates the difference between placing a series terminator near the source, which is common, and at the far end near the load, which is generally not advised. Both placements serve to absorb reflections before they can propagate along the trace multiple times. However, the far-end termination tends to produce more waveform distortion, while the near-end termination results in a cleaner signal. Additionally, parallel termination may be required to address VTT pull-up. These are typically placed at the end of a daisy chain to pull the signal up to VTT, the reference voltage for DDR2. Proper placement at the end of the line is essential.




▲ **Figure 3: Difference between the series terminator at the source and load.**

Effective component placement is essential for maintaining high-speed signal integrity, efficient power distribution, thermal management, and ease of manufacturing. Coordinate this with stackup planning, which determines routing paths, impedance levels, and return current behavior. Some tools offer precise dielectric control to facilitate optimal placement of critical components like clocks, SerDes, and DDR memory, reducing stub lengths, skew, and via count. Segregating nets based on voltage, rise time, and function—using route fences and signal layer keep-outs—helps mitigate crosstalk and EMI. Additionally, managing component

spacing to control flight time ensures timing consistency across clock domains. Proper placement of terminators and power decoupling components, particularly within DDR interfaces, further improves signal quality and overall system reliability.

## Key Points

- Establish the layer stack first. Use the stackup to decide where sensitive nets should live, then place components to ensure clean transitions between those layers.
- Partition component groups based on rise-time and operating frequency, positioning the highest-speed devices closest to the connector.
- All analog signals are routed within the analog section, while digital signals are confined to the digital section, both sharing a continuous common ground plane.
- Use keep-out zones across signal layers, effectively guiding the routing process and preventing signals from crossing designated boundaries on specific layers.
- Segregate groups of nets based on their signal amplitudes.
- Signal flight time and skew are critical considerations in high-speed PCB design.
- By controlling the placement of devices, the maximum signal delay can be approximated by the longest Manhattan (X + Y) distance within a specific clock domain.
- The clock should always have the longest delay so the data and address lines have time to settle before being clocked.
- Timing specifications and simulation results guide the establishment of placement and routing constraints.
- The DDR circuitry region must be isolated from other signals to prevent interference while maintaining a common ground plane.
- The recommendation is to locate these terminators within 200 mils of the signal source. **DESIGN007**

***Resources***

Beyond Design by Barry Olney: "Critical Placement," "The Fundamental Rules of High-Speed PCB Design Part 2," "Interactive Placement and Routing Strategies."

**Barry Olney** is managing director of In-Circuit Design Pty Ltd (iCD), Australia, a PCB design service bureau that specializes in board-level simulation. The company developed the iCD Design Integrity software, incorporating the iCD Stackup, PDN, and CPW Planner. You can download the software at www.icd.com.au. To read past columns, click here.

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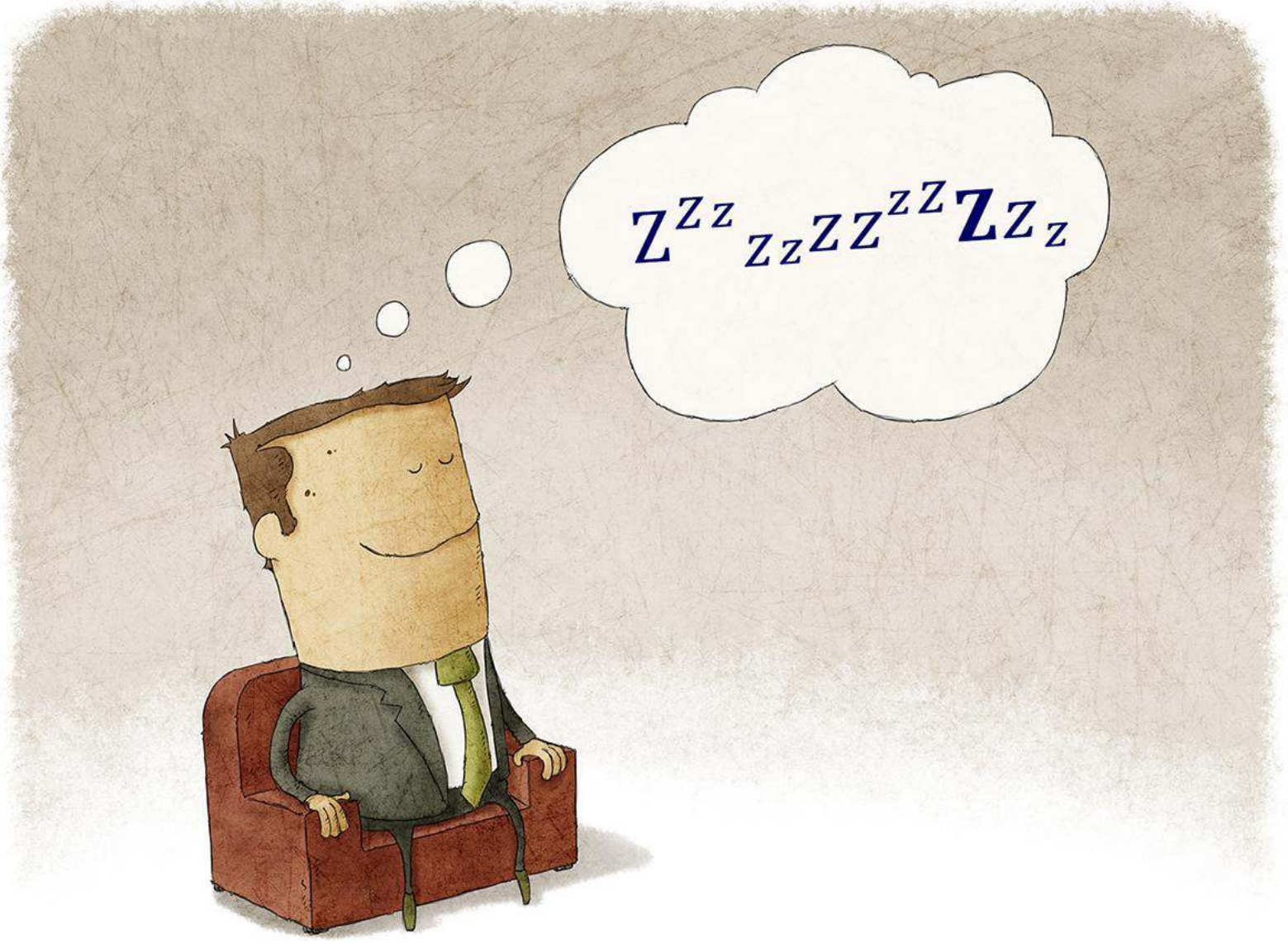


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