

iCD Design Integrity

incorporates the iCD Stackup and PDN Planner software. Offers PCB Designers unprecedented simulation speed, ease of use & accuracy at an affordable price

Dielectric Materials Library
30,700 Rigid & Flex Materials to 100GHz

Termination Planner
Extracts IV Curves from IBIS Models
Calculates Series Terminator of the Distributed System Including Loads

iCD Stackup Planner - Offers Engineers & PCB Designers unprecedented simulation speed, ease of use and accuracy at an affordable price

- Industry Leading 2D (BEM) Field Solver precision
- Characteristic impedance, edge-coupled & broadside-coupled differential impedance
- Relative Signal Propagation with 'Matched Delay Optimization'—ideal for DDRx design
- Termination Planner - series termination based on IBIS models & distributed system
- Unique Field Solver computation of multiple differential technologies per signal layer
- Extensive Dielectric Materials Library –over 30,700 rigid & flexible materials up to 100GHz
- Interfaces—Allegro, Altium, Excel, HyperLynx, OrCAD, PADS, Zmetrix TDR, Zuken & PC-2581B

iCD PDN Planner - Analyze multiple power supplies to maintain low AC impedance over entire frequency range dramatically improving product performance

- Fast AC impedance analysis with plane resonance and projected EMI
- Definition of plane size, dielectric constant & plane separation
- Extraction of plane data from the integrated iCD Stackup Planner
- Definition of voltage regulator, bypass/decoupling capacitors, mounting loop inductance
- PDN EMI Plot with FCC, CISPR & VCCI Limits. Frequency range up to 100GHz
- Extensive Capacitor Library –over 5,650 capacitors derived from SPICE models

“iCD Design Integrity software features a myriad of functionality specifically developed for high-speed design.”
- Barry Olney



FPGA PCB Design Challenges

by Barry Olney

IN-CIRCUIT DESIGN PTY LTD / AUSTRALIA

Field programmable gate arrays (FPGAs) are now commonplace in the majority of digital designs. These high-speed, high-gate/pin count devices, that once only provided glue logic, are now offering embedded processors, digital signal processors (DSPs), memory blocks and numerous input/output (I/O) pins in one massive ball grid array (BGA) package. Not to mention the considerable number of power supplies that are required to power the device. This added complexity has introduced many PCB layout challenges—apart from the obvious fanout and route of the fine pitch BGA. The reason for this added complexity is that EDA design tools have not kept pace with the growth in FPGAs. Rudimentary PCB layout tools were developed for designing PCBs, containing components with non-programmable pins such as processors and application specific integrated circuits (ASICs), and may not be suitable to FPGA integration.

The primary issue is generating optimal FPGA pin assignments that do not add vias and signal layers to a PCB stackup or increase the time required to integrate the FPGA with the PCB. Engineers generally do not consider FPGA pin assignments that expedite the PCB layout. Hundreds of logical signals need to be mapped to the physical pin-out of the device, and they must also harmonize with the routing requirements whilst maintaining the electrical integrity of the design.

To further frustrate the situation, FPGA I/O assignment is typically in a constant state of flux throughout the design process. Consequently, many PCB designs must be reiterated simply because the board and the FPGA design teams did not have the I/O pin-out synchronized. This has happened to me in the distant past. The board may go through the process of pre-layout simulation, place and route and then a post layout simulation, to verify all the timing is perfect, only to find on testing, the assembly, that the FPGA I/O pin-out is incorrect on the BGA footprint—damn! Meanwhile, days later, I had rerouted, run design rule checks, resimulated the layout and exported the deliverables.

Also, from a PCB layout point of view, crossovers of the connections should be minimized to give the router the best possible chance of completion. No matter how good the routing technology, crossovers will generally require two more vias per connection and hence more signal layers to route.

One should consider:

- Reducing the number of vias to minimize signal inductance, thus transmitting and receiving the signal at a higher quality
- Keeping the trace length of signals to a minimum to reduce transmission line losses, thereby improving signal quality

Figure 1 shows the rather disorganized I/O connections of a first pass FPGA pin assignment. This is typically what a PCB designer

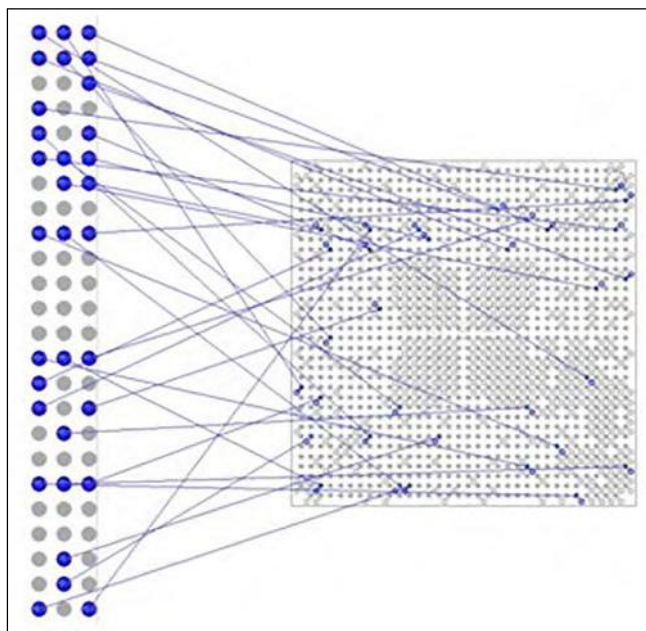


Figure 1: The dispersed connections need to be optimized to eliminate crossovers.

(All diagrams courtesy of Mentor Graphics.)

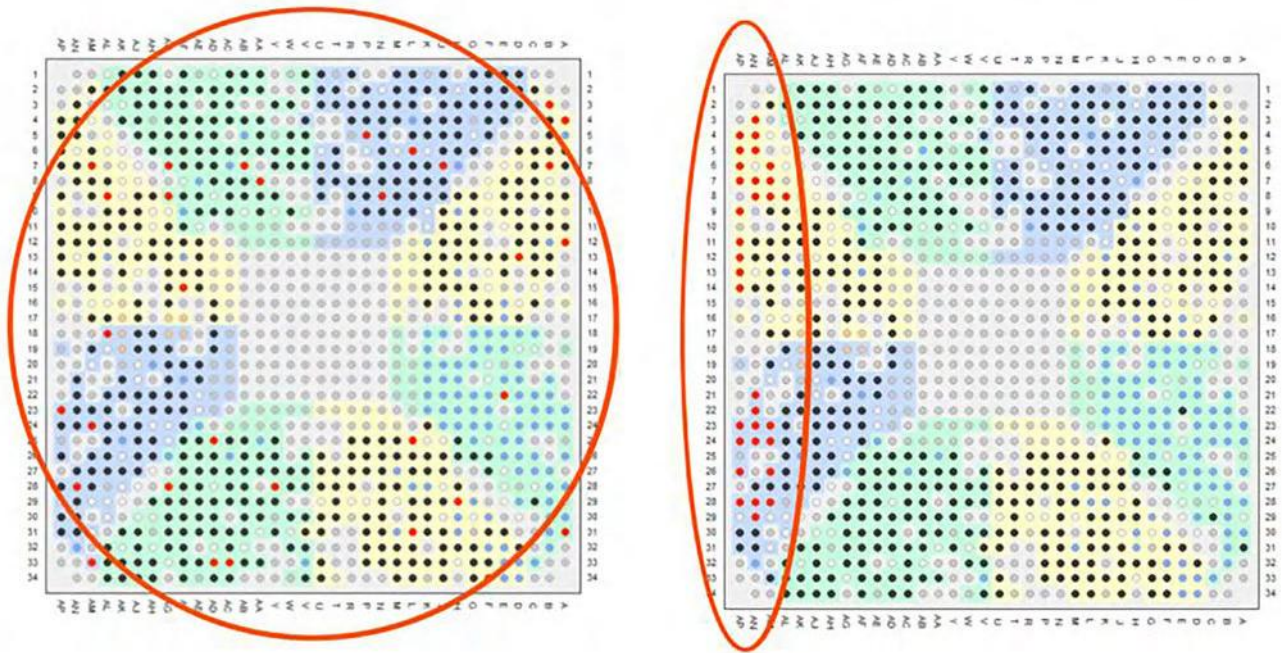


Figure 2: Original pin assignment (left) and modified pin assignment (right). Red is the I/O.

has to deal with, straight from the FPGA place and route tools. To make this more routable, the designer needs to adjust the pin assignment to firstly, be on one outer edge of the BGA. And secondly, order the pins to eliminate crossovers.

The connections in Figure 3 use the modified pin assignments displayed in Figure 2 which eliminates the crossovers making the FPGA I/O signals much easier to route, with fewer vias and fewer layers. This in turn improves the system performance, reduces manufacturing costs and time to market.

The problem now is how to back annotate this modified BGA pin assignment to the FPGA design tools? The manual process is time consuming, tedious and error prone. The key issue is to ensure consistency between the tool sets used in the hardware description language (HDL), FPGA and PCB environments. The language-based HDL representation of the FPGA must be properly represented as a schematic symbol containing the correct pin data, as well as the appropriate mapping to the BGA footprint.

Alternatively, I/O optimization tools can provide parallel paths of FPGA and PCB design, trimming weeks from the design process and

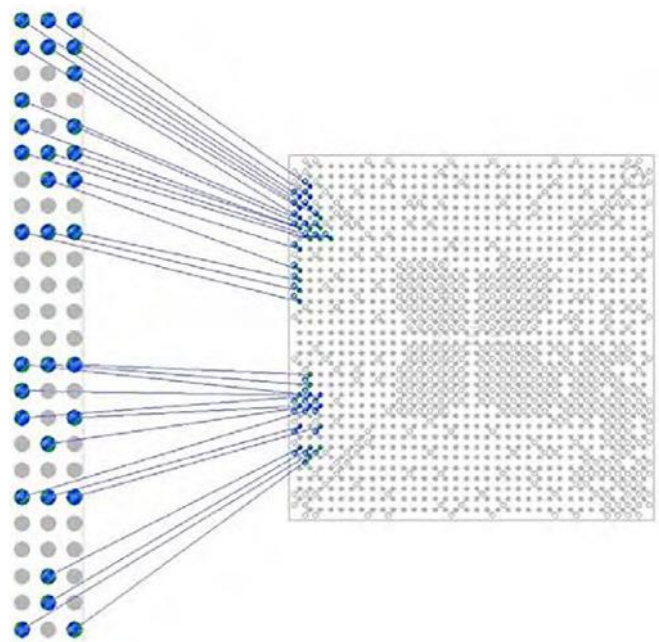


Figure 3: Crossovers are eliminated by modifying the pin assignment.

implementation schedules and providing significant overall cost benefits in the long term. These challenges can be met with such tools as Mentor Graphics' FPGA-PCB optimization

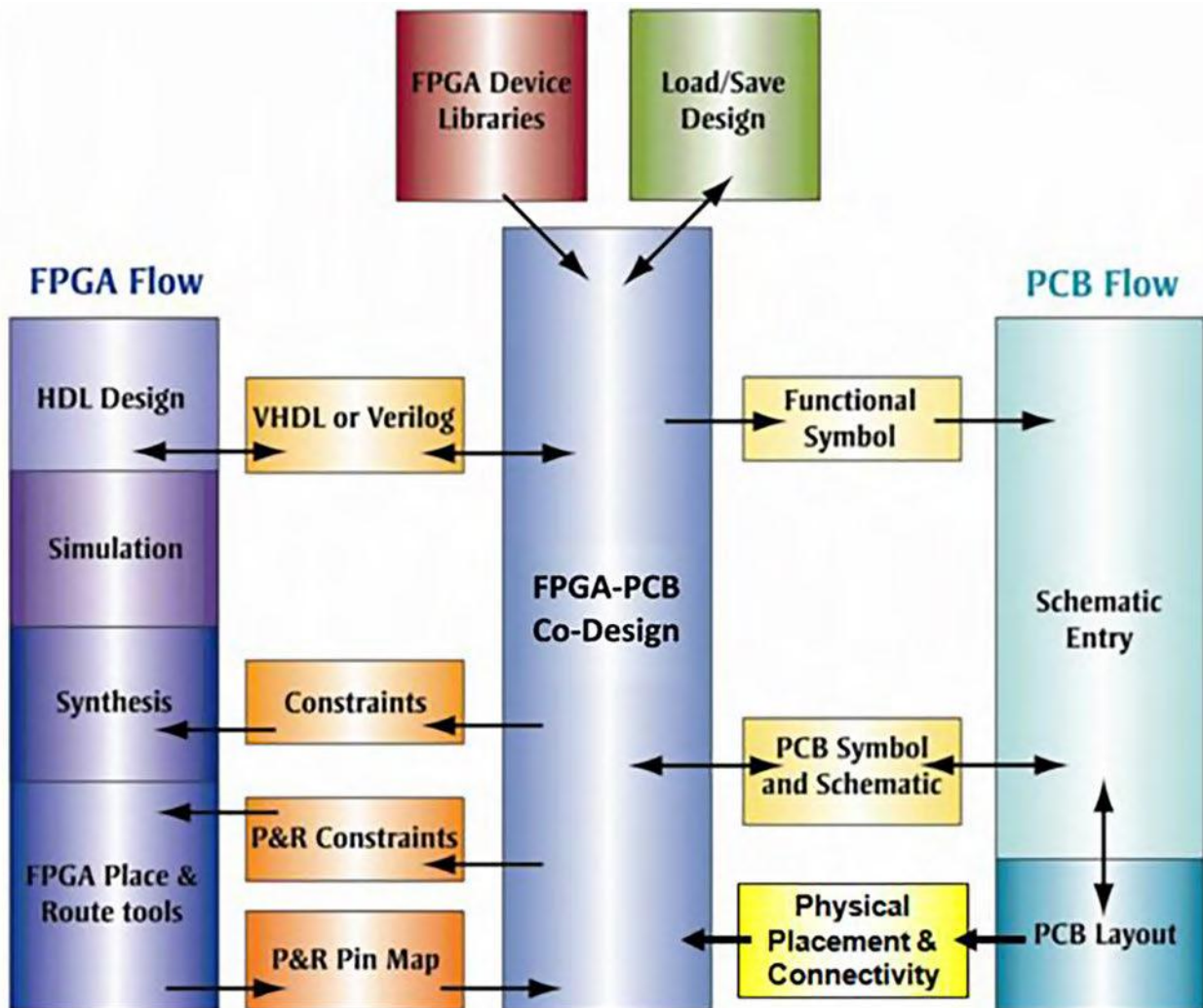


Figure 4: Synchronizing the FPGA and PCB flows.

technology that adds hardware description language (HDL) synthesis and advanced FPGA-PCB I/O optimization to PADS Professional software. This interface, between the HDL design environment and the physical implementation on the PCB, significantly reduces both time to market and manufacturing costs by automating the process, reducing errors and thus iterations.

Figure 4 illustrates the synchronization process. Essentially, once the FPGA design is completed, the pin assignment from the place and route tool is exported to the FPGA-PCB Co-Design software. A schematic symbol is automatically generated, with this pin assignment, and added to the schematic. The completed schematic is then forward annotated to the PCB

layout software. The BGA pin assignments can then be optimized to eliminate cross-overs and then back annotated, via the interface, to the FPGA tools. This synchronizes the FPGA pin assignment to that of the BGA footprint.

I/O optimization needs to be tightly integrated with the PCB design flow and be accessible at any stage of the project. Schematic, PCB layout and FPGA databases should always be synchronized which provides user control of the project's design data flow.

An FPGA vendor-neutral design environment that enables architecture-specific optimization takes advantage of the specific features for each FPGA device to meet the design requirements. Vendor-independent synthesis supports

devices from Altera, Lattice, Microsemi, and Xilinx. Therefore, you may use the same HDL design source files and constraints to target any device and to obtain a synthesized netlist that can be used for place and route with the appropriate vendor tools. This vendor independence, allows users to easily retarget and analyze results for any FPGA device, enabling you to find the best FPGA device to suit the design.

Until recently, the FPGA-PCB I/O optimization tools were expensive and only available with enterprise level flows such as Cadence Allegro and Mentor Xpedition, but are now also an affordable option to the PADS Professional suite of PCB design tools. Automating the error-prone boundary between FPGA and PCB design makes sense. Design teams need to implement new methodologies to ensure they do not negate the cost and time-to-market benefits of using programmable logic in the first place.

Points to remember:

- The added complexity of FPGA integration has introduced many PCB layout challenges.
- EDA design tools have not kept pace with the growth in FPGAs.
- The primary issue is generating optimal FPGA pin assignments that do not add vias and signal layers to a PCB.
- FPGA I/O assignment is in a constant state of flux.
- Cross-overs of the rat's nest should be minimized to give the router the best possible chance of completion.
- The problem now is how to back annotate this modified FPGA pin assignment to the FPGA design tools.

- The manual process is time consuming, tedious and error prone.

- The key issue is to ensure consistency between the tool sets used in the FPGA and PCB environments.

- Using the right tools can provide parallel paths of FPGA and PCB design, trimming weeks from the design process and implementation schedules.

- Schematic, PCB layout and FPGA databases should always be synchronized which provides user control of the project's design data flow.

- An FPGA vendor neutral design environment, which enables architecture-specific optimization, takes advantage of the specific features for each FPGA device. **PCBDESIGN**

References

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3. I/O Optimization: Mentor Graphics, PADS literature.
4. FPGA-PCB Co-Design Option for PADS Professional: Mentor Graphics, PADS literature.



Barry Olney is managing director of In-Circuit Design Pty Ltd (iCD), Australia, a PCB design service bureau that specializes in board-level simulation. The company developed the iCD Design Integrity software incorporating the iCD Stackup, PDN and CPW Planner, available for download at www.icd.com.au.

New Technique Enables 3D Printing with Paste of Silicone Particles in Water

In a paper published today in *Advanced Materials*, corresponding author Orlin Velev and colleagues show that, in a water medium, liquid silicone rubber can be used to form bridges between tiny silicone rubber beads to link them together – much as a small amount of water can shape sand particles into sandcastles.

"There is great interest in 3D printing of silicone rubber, or PDMS, which has a number of useful properties," said Velev, INVISTA Professor of Chemical and Biomolecular Engineering at NC State. "The challenge is that you generally need to rapidly heat the material or use special chemistry to cure it, which can be technically complex."