

The Eye Diagram

Beyond Design

by Barry Olney, IN-CIRCUIT DESIGN PTY LTD / AUSTRALIA

An eye diagram is a useful tool for the analysis of signals used in digital transmission. It provides a quick scan of system performance and can offer insight into the nature of channel imperfections. An eye diagram is simply a graphical display of a serial data signal with respect to time that shows a pattern that resembles an eye. Careful scrutiny of this visual display can give one a first-order approximation of signal-to-noise, clock timing jitter, reflections and skew. In this month's column, I will take an eye-ball look at the eye diagram.

An eye diagram overlays the signal waveform over many cycles. The stimulus is normally a pseudo-random bit stream (PRBS). Each cycle waveform is aligned to a common timing reference, typically a clock. An eye diagram provides a visual indication of the volt-

age and timing uncertainty associated with the signal. In an ideal world, eye diagrams would look like rectangular boxes. However, in reality, communications are not perfect, so the transitions do not align perfectly, resulting in an eye-shaped pattern.

A pseudo-random bit stream is a program that applies mathematical algorithms to simulate randomness. It generates a sequence of binary numbers, synchronized by a clock, approximating the properties of random numbers. The triggering edge may be positive or negative, but the resultant pulse that appears after a delay period may go either way. Therefore, when many such transitions are overlaid, positive and negative pulses are superimposed on each other. Overlaying many such bits produces an eye diagram. This sequence (up to

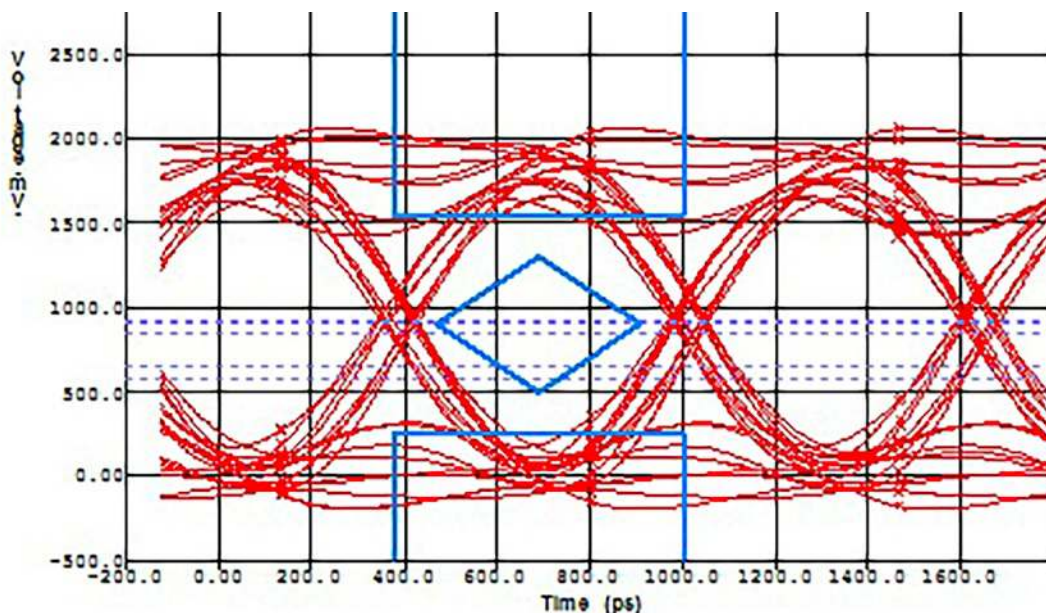


Figure 1: Eye diagram of a serial data stream with an eye mask.

1024 bits/s) is used to stimulate IBIS models in a transmission line configuration and, at the receiver, results in an eye diagram that visualizes the signal quality. To get a quantitative view of signal integrity performance, other measurements can be applied to the eye-diagram pattern, including eye height, eye width, signal amplitude, comparative delay, slew rate and setup/hold times. The measured values can then be compared with the JEDEC specification.

The quality of a high-speed digital signal can be quickly determined by using a compliance mask overlay on the eye diagram display (Figure 1). A typical mask includes both time and amplitude limits. The blue area is keep-out.

The mask template can be configured based on the JEDEC specification, in which the middle section of the mask is made up of the setup/hold time and stable voltage threshold specifications. Masks can also be customized to test certain specifications. By applying a mask test to the eye diagram, one can quickly tell if the signal can meet the overall signal integrity requirement. Unfortunately, mask dimensions are often difficult to determine from the specifications.

Eye diagrams include voltage and time samples of the data acquired at some sample

rate below the data rate. In Figure 2, the bit sequences (left) are superimposed over one another to obtain the final eye diagram (right).

What an eye diagram (Figure 3) can tell us:

- AC timing noise or jitter, which is indicated by horizontal thickness
- AC noise or reflections, which is indicated by vertical thickness of the bunches
- The unit interval or symbol duration, which is equivalent to the center-to-center spacing of the crossovers
- The peak-to-peak voltage
- Overshoot and undershoot above/below the peak-to-peak waveform
- Whether the ring back is above or below the peak-to-peak waveform
- Rise/fall time, which can be measured from 10% to 90% of the rising/falling edge
- The comparative delay between two or more signals

Jitter arises when a rising or falling edge occurs at times that differ from the ideal. Some edges occur early; some occur late. In a digital circuit, all signals are transmitted with reference to a clock signal. The deviation of the digital signals as a result of reflections, inter-

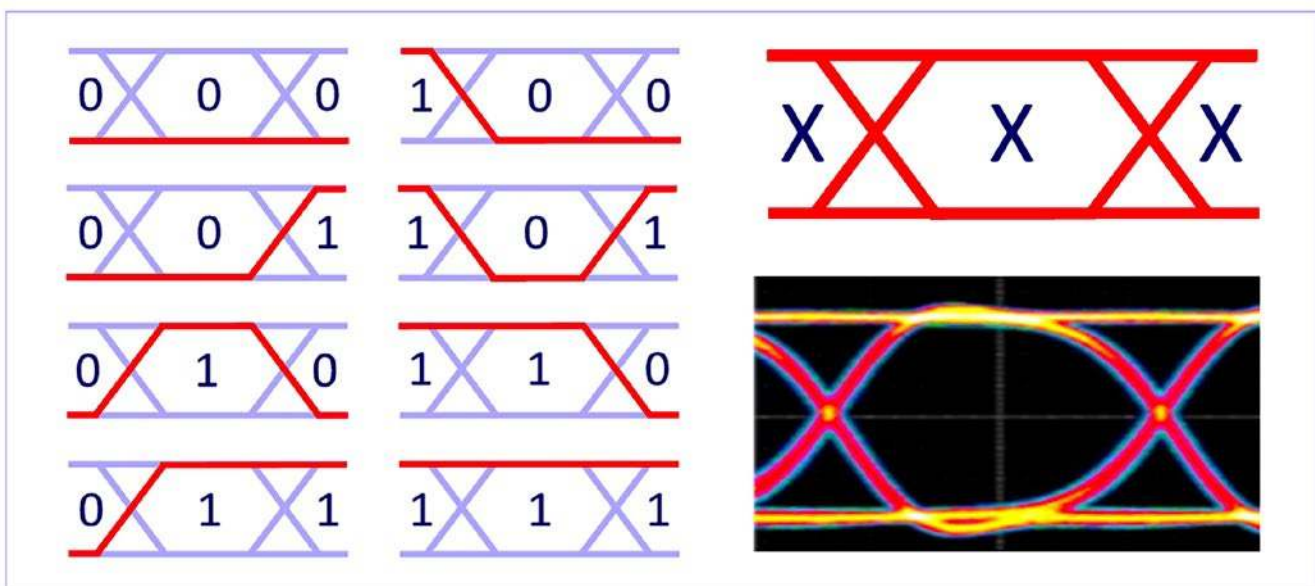


Figure 2: Formation of an eye diagram.

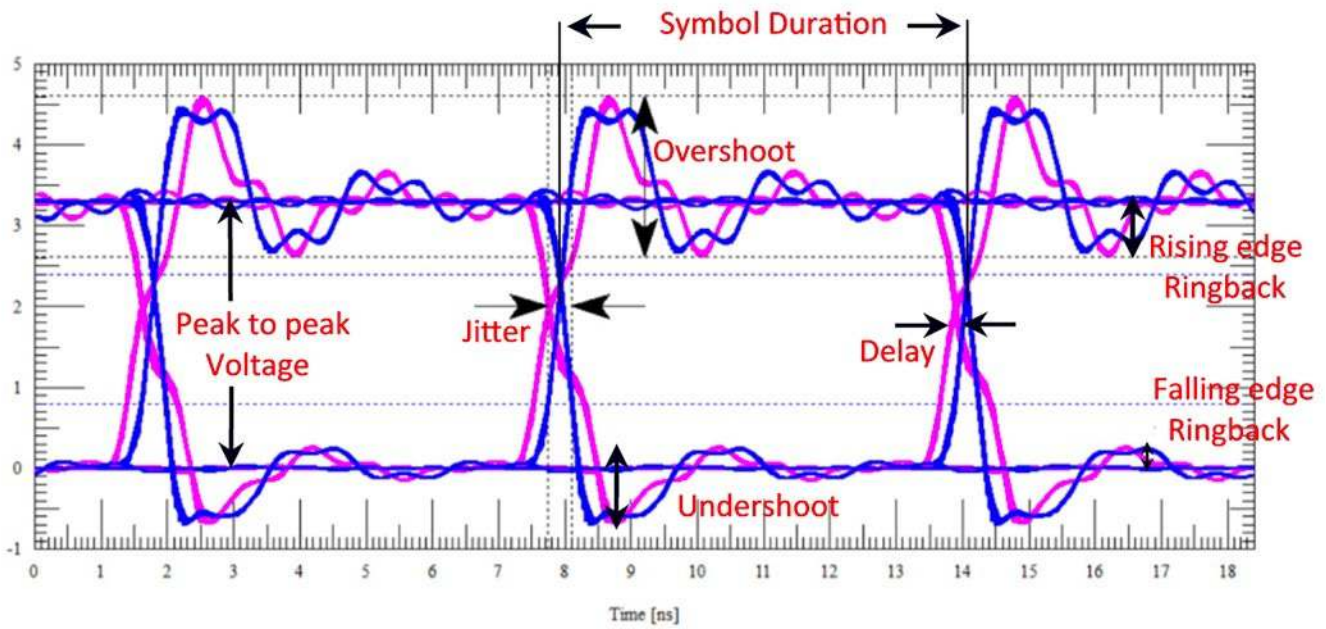


Figure 3: Eye diagram measures signal quality.

symbol interference, crosstalk, process-voltage-temperature variations, and other factors amounts to jitter. Some jitter is simply random.

The impact of termination is clearly visible in the eye diagrams generated. With improper termination, the eye looks constrained or stressed; with improved termination schemes, the eye becomes more relaxed (open). A poorly terminated signal line also suffers from multiple reflections.

A practical way to analyze DDR signals is via the eye diagram. Either read or write DQ is folded into an eye based on the reference clock recovered from the DQS strobe edge. A composite eye diagram can tell the exact jitter content and distribution in your memory

interface, as the DQ signals are referenced to a clock (strobe signal). Additionally, it can display reflections from incorrect driver selection and on-die-terminations (ODT), as in Figure 4. Variations (reflections) at the peaks on the waveform indicate inappropriate termination.

Eye diagrams can also pickup stubs on high-speed serial links. Figure 5 shows the effects of excessively long via stubs on a high-speed differential pair. On the left, the differential pair is simulated using a pseudo-random bit stream with lossy transmission lines enabled—note the open-eye pattern. However, on the right, I have included via modelling, which enables the via parasitics and highlights the effects of via resonance. The high frequency harmonics

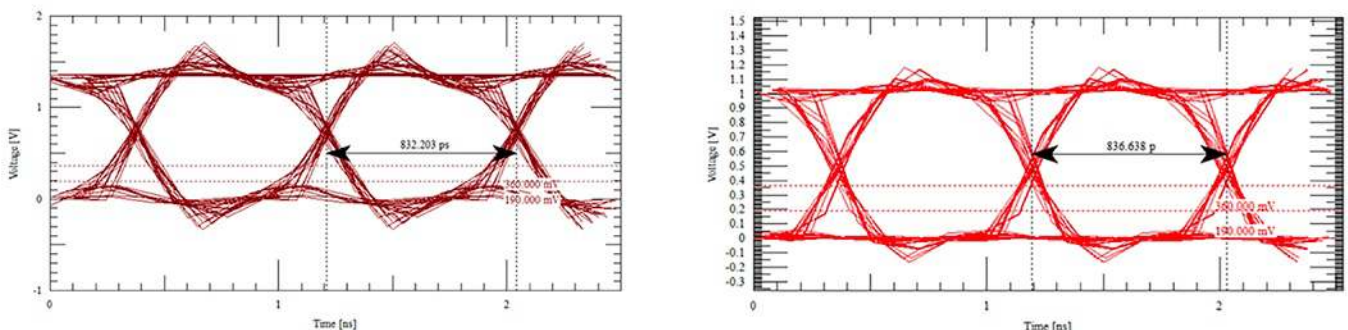


Figure 4: DDR3 data streams. 40Ω driver withno ODT (left); 40Ω driver with 80Ω ODT (right).

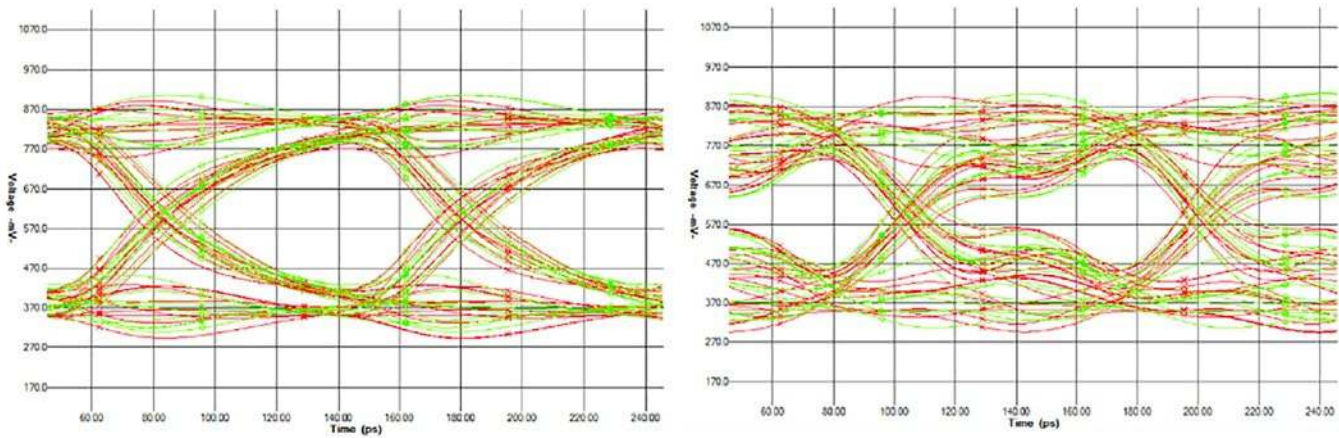


Figure 5: High-speed 10Gbps. Ethernet differential signal (left), and with via resonance (right).

are attenuated, rolling off the signal rise time, distorting the signal, reducing bandwidth, and closing the eye.

Reflections are reduced dramatically by eliminating the stub. Back-drilling the via stub is a common practice on thick PCBs to minimize stub length for bit-rates greater than 3Gbps (1.5GHz). However, at transmission rates >10Gbps (5GHz), back-drilling alone may not be adequate to reduce jitter and bit error rate.

Eye diagram analysis is not the same as a bit error rate (BER) analysis, but the two techniques are often used in conjunction. The bit error rate percentage is calculated as the number of bit errors per unit of time. Bit synchronization errors are a factor, as well as distortion, interference, and noise.

The eye pattern is a composite signal that indicates the channel bandwidth, attenuation, jitter, reflections, comparative delay, and rise/fall time variations. Eye pattern measurements can show the overall signal integrity of a data path. They provide instant visual data that digital designers can use to check the signal integrity of a design and uncover problems early in the design process.

Key Points

- An eye diagram provides a visual indication of the voltage and timing uncertainty associated with the signal.

- The stimulus is normally a pseudo-random bit stream. Each cycle waveform is aligned to a common timing reference, typically a clock.
- Overlaying many bits produces an eye diagram.
- The quality of a high-speed digital signal can be quickly determined by using a compliance mask overlay.
- The eye mask is made up of the setup/hold time and stable voltage threshold specifications.
- Jitter arises when a rising or falling edge occurs at times that differ from the ideal.
- The impact of termination is clearly visible in the eye diagrams generated.
- A practical way to analyze DDR signals is via the composite eye diagram.
- A composite eye diagram can tell the exact jitter content and distribution in your memory interface, as the DQ signals are referenced to the strobe signal.
- Reflections at the peaks on the waveform indicate inappropriate termination.
- Eye diagrams can also pick stubs on high-speed serial links.
- Back-drilling the via stub is a common practice on thick PCBs to minimize stub length for bit-rates greater than 3Gbps (1.5GHz).

- Bit error rate is calculated as the number of bit errors per unit of time. **DESIGN007**

- *Signal and Power Integrity – Simplified*, by Eric Bogatin, Jan. 2019.

Resources

- “Beyond Design: How to Handle the Dreaded Dangers, Part 2,” by Barry Olney, *PCBDesign007 Magazine*, Sept. 2016.
- “Fly-over Technology – When It All Gets Too Fast,” by Barry Olney, *PCBDesign007 Magazine*, Aug. 2021.
- “Eye diagram basics: Reading and applying eye diagrams,” by Deepbak Behera, et al., *EDN.com*, Dec. 16, 2011.
- “What Is a High-Speed Eye Diagram?” by Texas Instruments Precision Labs, *ti.com*, 2019.



Barry Olney is managing director of In-Circuit Design Pty Ltd (iCD), Australia, a PCB design service bureau that specializes in board-level simulation. The company developed the iCD Design

Integrity software incorporating the iCDStackup, PDN, and CPW Planner. The software can be downloaded at www.icd.com.au. To read past columns, [click here](#).

At the Edge of Graphene-Based Electronics

A pressing quest in the field of nanoelectronics is the search for a material that could replace silicon. Graphene has seemed promising for decades. But its potential faltered along the way, due to damaging processing methods and the lack of a new electronics paradigm to embrace it. With silicon nearly maxed out in its ability to accommodate faster computing, the next big nanoelectronics platform is needed now more than ever.

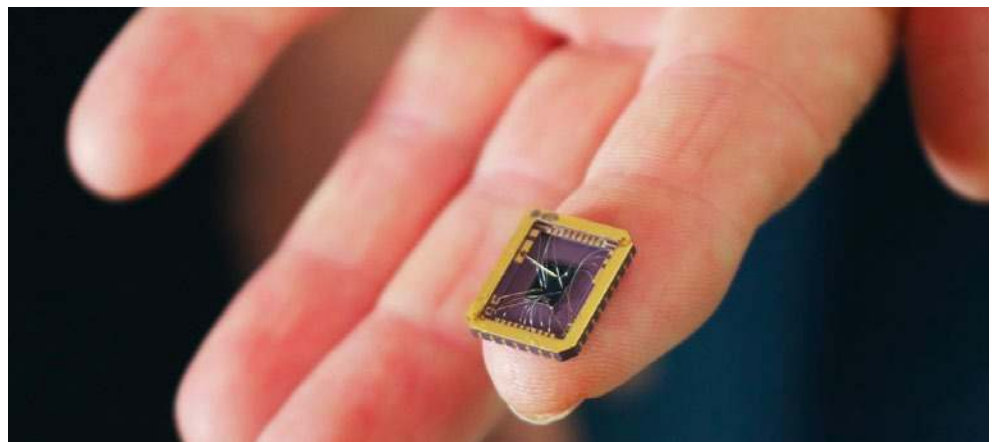
Walter de Heer, Regents' Professor in the School of Physics at the Georgia Institute of Technology, has taken a critical step forward in making the case for a successor to silicon. De Heer and his collaborators developed a new nanoelectronics platform based on graphene—a single sheet of carbon atoms. The technology is compatible with conventional microelectronics manufacturing, a necessity for any viable alternative to silicon. Their discovery could lead to manufacturing smaller, faster, more efficient, and more sustainable computer chips, and has potential implications for quantum and high-performance computing.

To create the new nanoelectronics platform, the researchers created a modified form of epitaxial graphene on a silicon carbide crystal substrate. In collab-

oration with researchers at the Tianjin International Center for Nanoparticles and Nanosystems at the University of Tianjin, China, they produced unique silicon carbide chips from electronics-grade silicon carbide crystals. The graphene itself was grown at de Heer's laboratory at Georgia Tech using patented furnaces.

This process mechanically stabilizes and seals the graphene's edges, which would otherwise react with oxygen and other gases that might interfere with the motion of the charges along the edge.

It will likely be another five to 10 years before we have the first graphene-based electronics, according to de Heer. But thanks to the team's new epitaxial graphene platform, technology is closer than ever to crowning graphene as a successor to silicon.

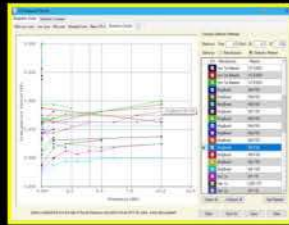


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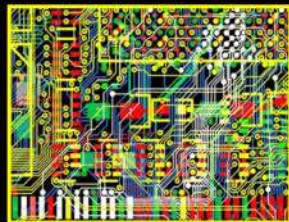


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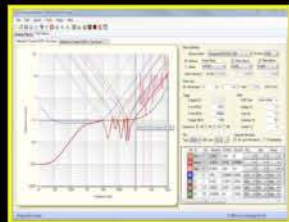
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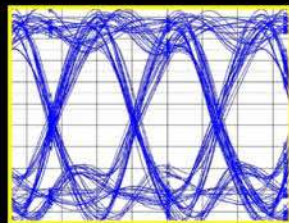
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