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Embedded Signal Routing

by **Barry Olney**

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We hear all the time that one should avoid routing high-speed signals on the outer layers of a multilayer PCB. I myself preach this. Some say that this decreases radiation by up to 15 dB. But, how much attenuation do we actually get from embedding the high-speed signals between the planes?

The four constraints to keep in mind:

1. Keep the mark-to-space ration of the waveform equal as this eliminates all the even harmonics.
2. Route high-speed signals out from the centre of the board where possible as any radiation will be in the opposite direction and will tend to cancel.
3. Route high-speed signals between the planes, fanout close to the driver (200mil) dropping to an inner plane and route back up to the load again with a short fanout.
4. Use the same reference plane for the return signals as this reduces the loop area and hence radiation.

Embedding signals between the planes also reduces susceptibility to radiation, as well as providing ESD protection. So, not only do we prevent noise from being radiated, but we also reduce the possibility of being affected by an external source.

Unfortunately, the high-frequency components of the fundamental (lowest frequency in a complex wave) radiate more readily because their shorter wavelengths are comparable to trace lengths, which act as antennas. Consequently, although the amplitude of the

SUMMARY

Is radiation actually attenuated when high-speed signals are routed embedded between the planes? There are specific constraints and factors to consider when assessing just how much attenuation we actually get from embedding the high-speed signals between the planes.

harmonic frequency components decreases as the frequency increases, the radiated frequency varies depending on the antenna/trace characteristics. Typically, the 5th and 7th harmonics radiate the most.

Also, studies conducted by Hewlett Packard have found that there is up to 20 dB greater emissions from edge-located traces compared to traces located in the centre of the board on outer layers. Yet, the same test performed on buried traces indicated no change as the traces were placed nearer the PCB edges. From this, we gather that it is best to keep well away from the edge of the board when routing on the outer layers. The impedance changes as the reference plane decreases in area beneath the trace.

In order to measure the difference in radiation between an embedded signal and a signal routed on an outer layer, I have ripped up a DDR2 design that I recently did. Of course, I try to avoid routing on the other layers so I will have to make a few changes to measure the effects.

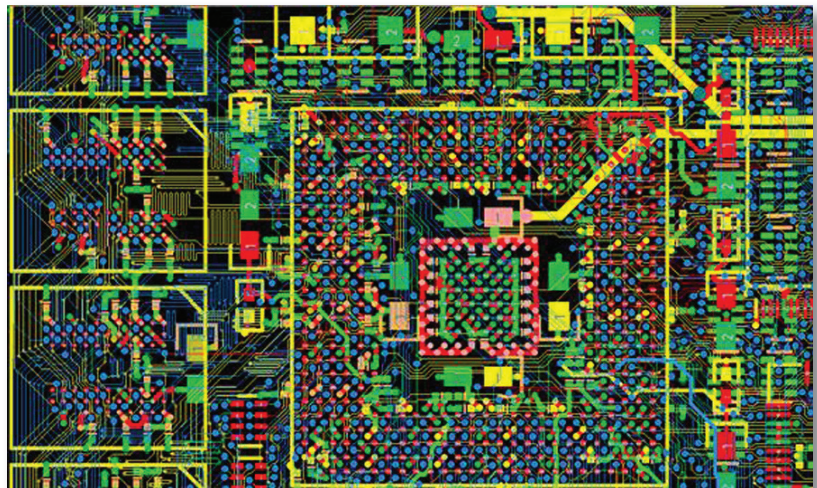


Figure 1. The layout of the DDR2 section of the board.

ICD STACKUP PLANNER – www.icd.com.au 5/23/2011 Total Board Thickness: 57.2

Layer		Material	Dielectric		Copper	Trace		Current	Impedance	Edge Coupled	Broadside Coupled	Description
Number	Name	Type	Constant	Thickness	Thickness	Clearance	Width	(Amps)	Characteristic(Zo)	Differential(Zdiff)	Differential(Zdbs)	
1	Top	Dielectric	3.3	0.5	1.4	8	4	0.31	53.53	99.99		Soldermask
		Conductive										Signal
2	1/8 Plane	Dielectric	4.3	3	1.4							Prepreg
		Conductive										Plane
3	Inner 3	Dielectric	4.3	5	1.4	15	4	0.31	52.87	96.8		Core
		Conductive										Signal
4	3/3 Plane	Dielectric	4.3	9	1.4							Prepreg
		Conductive										Plane
5	GND	Dielectric	4.3	12	1.4							Core
		Conductive										Plane
6	Inner 6	Dielectric	4.3	9	1.4	15	4	0.31	52.87	96.8		Prepreg
		Conductive										Signal
7	0/9 Plane	Dielectric	4.3	5	1.4							Core
		Conductive										Plane
8	Bottom	Dielectric	3.3	0.5	1.4	8	4	0.31	53.53	99.99		Prepreg
		Conductive										Signal
		Dielectric										Soldermask

Figure 2. The multilayer stackup.

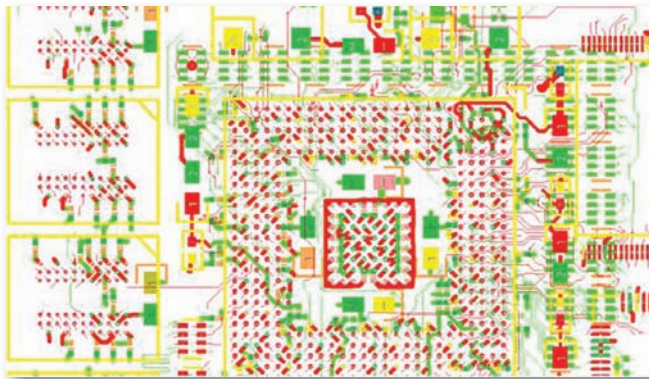


Figure 3. Very little routing is done on Layer 1 and 8 (outer layers). Fanout, then straight down to the embedded planes.

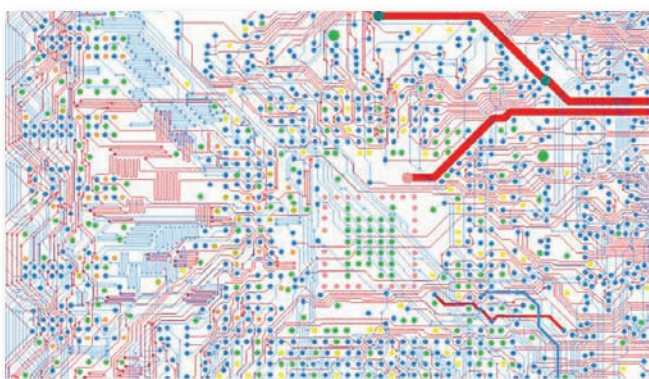
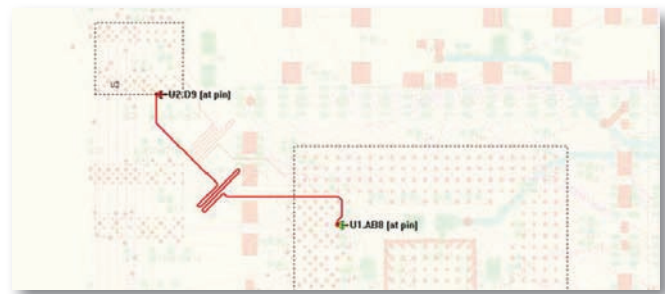


Figure 4. Layers 3 and 6 contain all the DDR signals. The data lanes, strobes, address and command signals are matched to length constraints.

As you can see from the design in Figure 1, the routing is very dense with serpentine, matched length traces connecting the DDR2



DDR MDQ5 layer 3

Figure 5. Data signals were rerouted on the outer (Top) layer. These signals are matched to 1.6 inch as per the previous connects.

memory to the CPU. DDR2 designs tend to radiate a fair bit anyway because of the close proximity of traces in a confined area.

The first thing to look at is the multilayer stackup. Characteristic impedance needs to be near 50 ohm and differential impedance around 100 ohms. The above is a very safe stackup, which I use all the time for this type of design. The impedance has been calculated by the ICD Stackup Planner (this can be downloaded from www.icd.com.au).

Why safe? Each layer is embedded between two planes, reducing crosstalk from adjacent layers and providing a clear return path for the signals.

The first red line (starting @ 40 dB) is the FCC Class B limit (the most stringent for residential and small office environments). The blue line is the CISPR Class B limit. Above those are the Class B limits, which are more

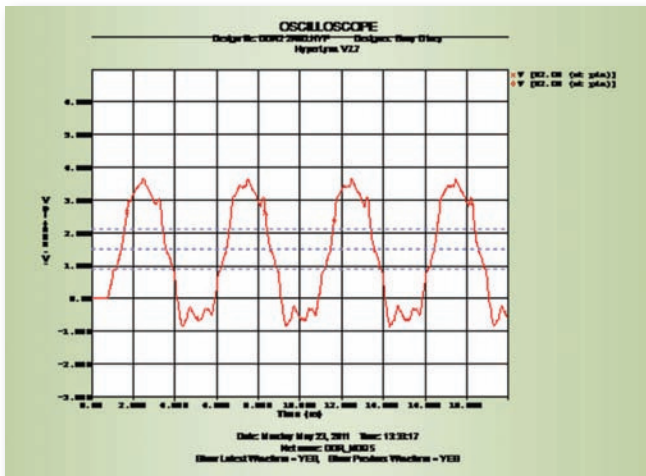


Figure 6. The waveform of DQ5 looks a little noisy on the bottom, but the skew is still pretty good and there are no non-monotonic edges near the trigger levels.

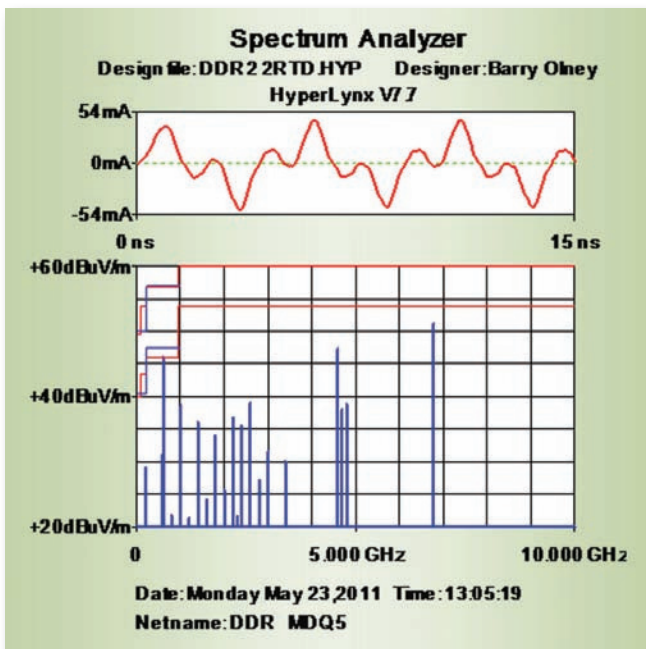


Figure 7. The radiation of DQ5 is displayed above in the virtual Spectrum Analyzer.

lenient for commercial environments. The third harmonic peaks at 46 dB just over the Class B limit. Currently, the FCC and CISPR limits only go up as far as 1 GHz but we can measure the higher harmonics up to 10 GHz.

Also of concern, are the higher harmonics with 45.65 dB, 4.595 GHz and 49.73 dB @ 6.76 GHz. This certainly would not pass the



Figure 8. DQ5 routed on inner layer 3.

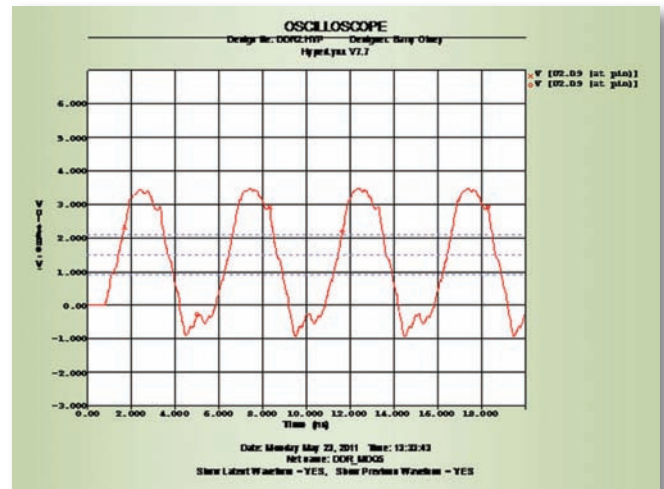


Figure 9. Again, the DQ5 signal looks pretty normal on the virtual oscilloscope. Not so much noise this time on the bottom of the waveform.

Electromagnetic Compliance (EMC) test.

Let's look now at the working design that actually passed the EMC. The original DQ5 trace is routed on the inner layer 3. As you can see, the fanout is very close to the driver and load so that the signal is almost totally embedded between the planes. In this case, we decided not to use series terminators (after pre-layout simulation) as the traces are short and it was not warranted.

Let's make a comparison of the radiated noise (see Figure 10).

As you can see (with all other factors being equal), in this case the trace routed on the inner layer 3 exhibits between 4 to 10 dB less noise than the trace routed on the top layer. Also, please note that there are more high harmonics on the top layer routing. The high-frequency components radiate more

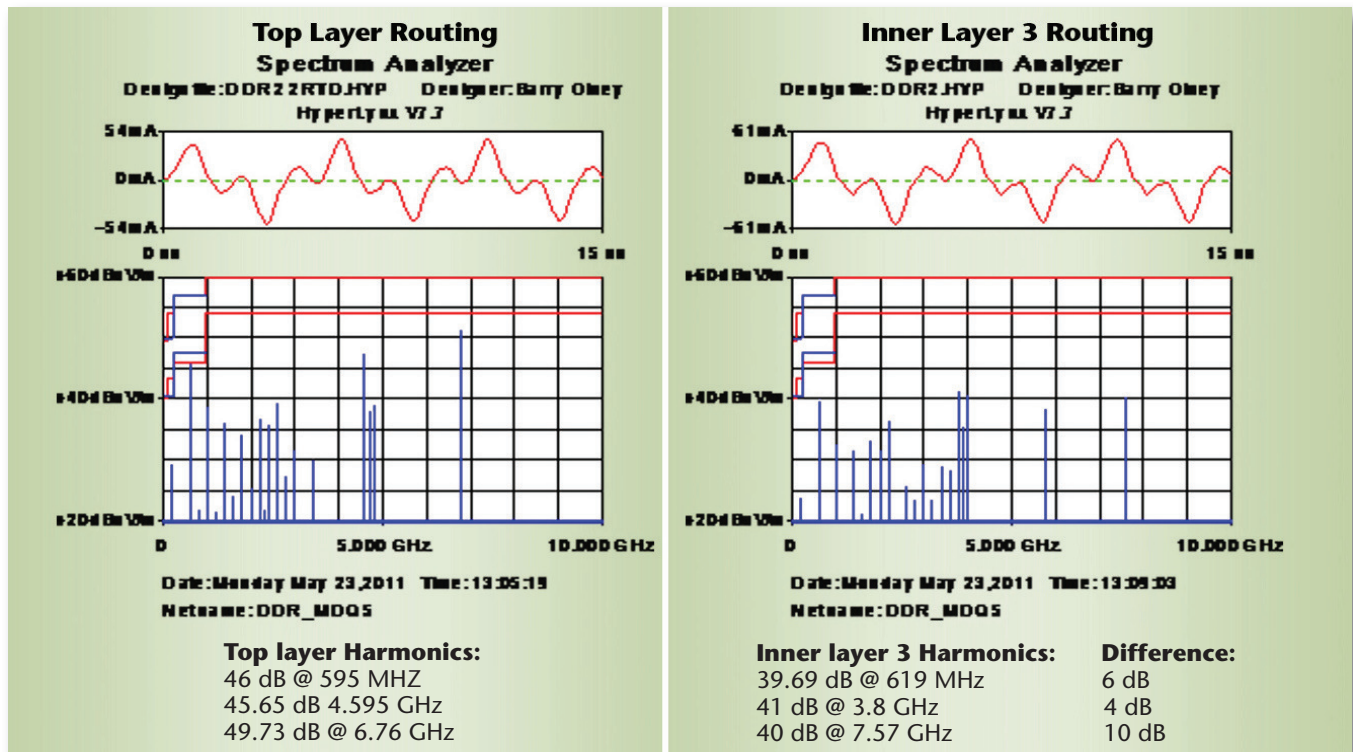


Figure 10.

readily because their shorter wavelengths are comparable to trace lengths, which act as antennas. Consequently, although the amplitude of the harmonic frequency components decreases as the frequency increases, the radiated frequency varies depending on the traces characteristics.

In conclusion, routing high-speed signals embedded between the planes does reduce the radiated emissions by as much as 10 dB (in this case). Adding a series terminator may help reduce this even further, but this should be determined by simulation and has to be a trade-off with other factors as in any design.

References:

1. Advanced Design for SMT – Barry Olney, In-Circuit Design Pty Ltd.
2. PCB Stack-up – Henry Ott Consultants.
3. ICD Stackup Planner – In-Circuit Design Pty Ltd (download from www.icd.com.au).

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