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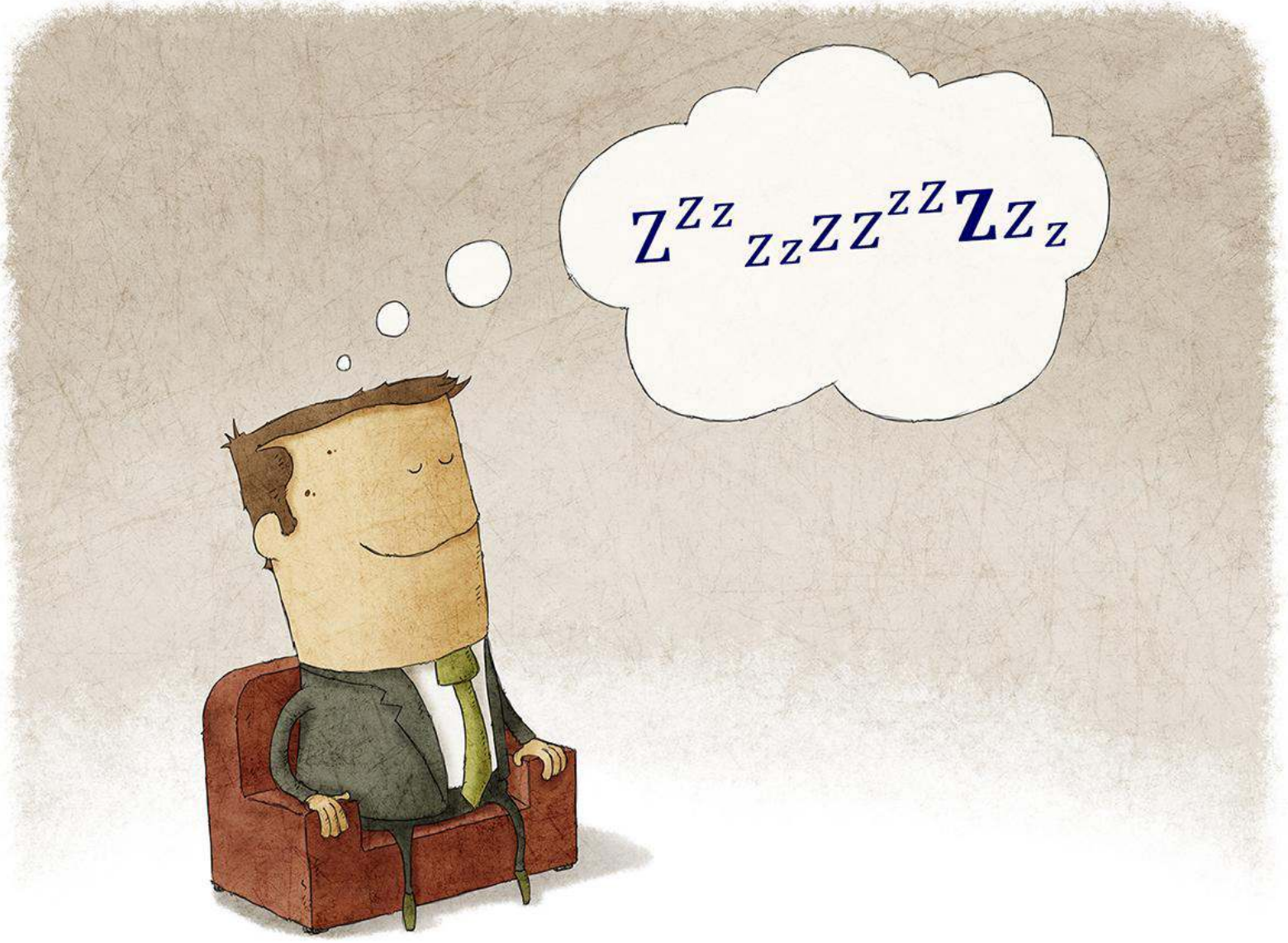

Did you know that two seemingly unrelated concepts are the foundation of a product's performance and reliability?

- Transmission line impedance and
- Power Distribution Network impedance

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Embedded Capacitance Material

Beyond Design

Feature Column by Barry Olney, IN-CIRCUIT DESIGN PTY LTD / AUSTRALIA

Embedding components into the multilayer PCB substrate can have many benefits, including reduced board size and improved signal integrity. However, embedded capacitance material (which is not really a component but rather part of the substrate) can improve power integrity dramatically by reducing AC impedance and generally enhancing the performance of the product. It takes up no additional space, is easy to implement (because it is compatible with standard FR-4 processes), and can be cost-effective.

A combination of components is generally required to optimize the power distribution network (PDN). Figure 1 shows how each component has a specific resonant frequency at which point the impedance will be low. The voltage regulator module (VRM), bulk bypass and decoupling capacitors, plane, die capacitance plus BGA via, and via spreading inductance all influence the PDN at different frequencies. The goal is to keep the AC impedance low over the entire signal bandwidth. However, decoupling capacitors are only effective up to a few hundred megahertz. Above that, only on-die capacitors or planar capacitance can reduce the impedance significantly due to their low inductance.

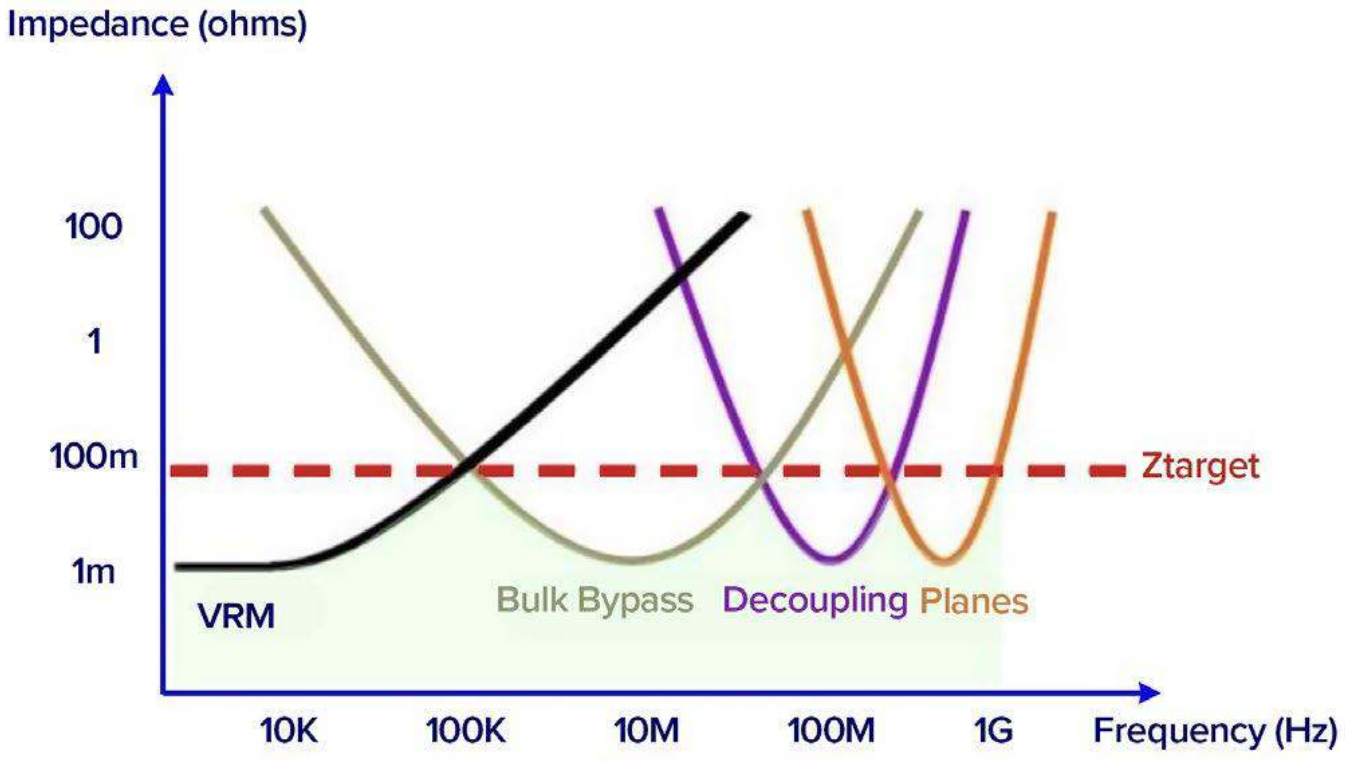


Figure 1: Target impedance, VRM, capacitor, and plane profiles of a PDN.

With the trend to smaller feature sizes and faster signal rise times, embedded capacitance material (ECM) is becoming a cost-effective solution to improve power integrity further. This technology provides an effective approach for decoupling high-performance ICs while reducing electromagnetic interference.

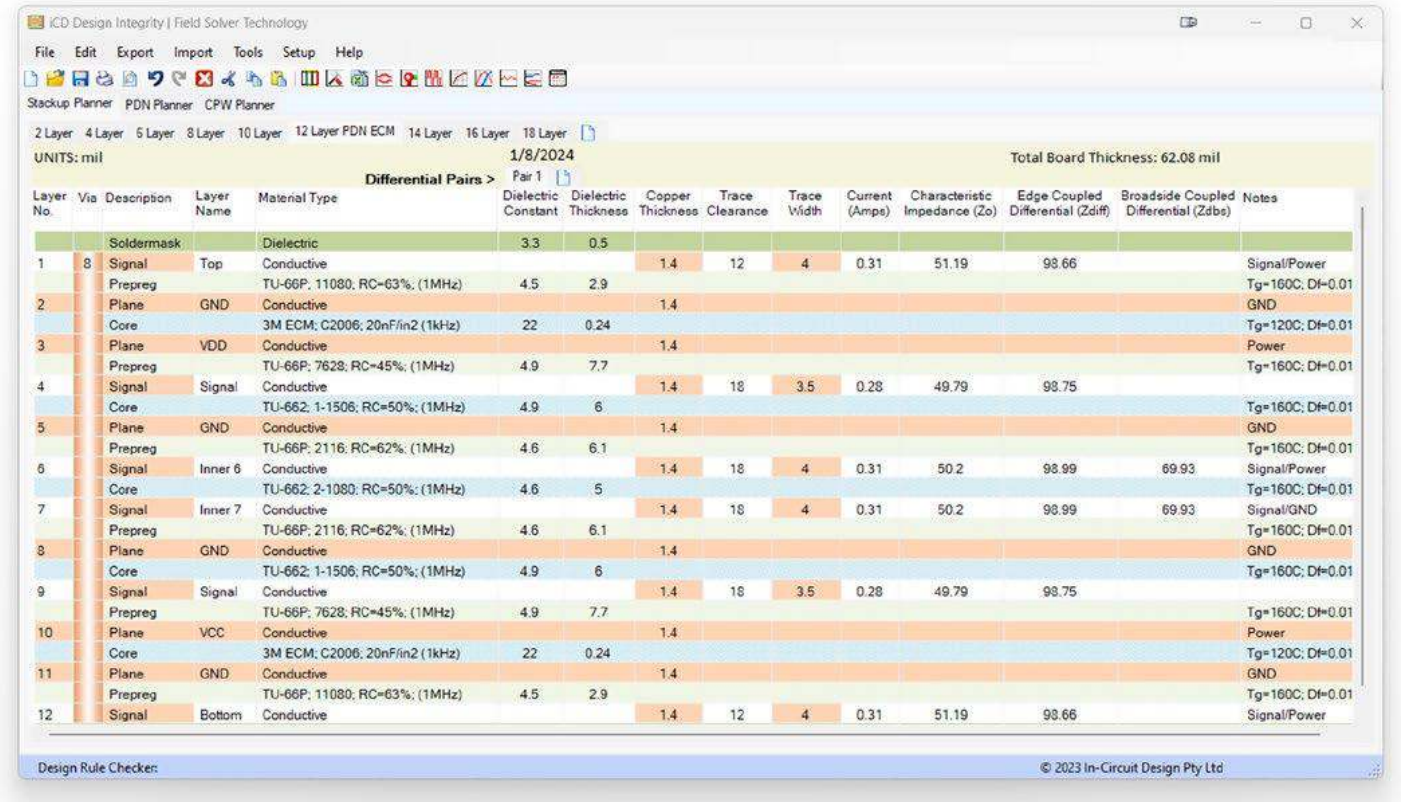
Plane pair cavity resonances contribute to emissions. Smaller plane separation implies less area of equivalent magnetic current at the plane pair edge, or equivalently less local fringing field volume, and therefore lower emissions for a given field strength. However, the smaller the plane separation, the higher the Q of the cavity can be, resulting in higher field strength at the plane pair edges.

Embedded capacitance material comprises copper-clad laminates with very thin dielectric thickness and high dielectric constant. These materials can replace the standard power and ground planes, thereby providing additional capacitance embedded into the PCB stackup. Embedded capacitance materials are defined and described in IPC 4821, *Specification for Embedded Passive Device Capacitor Materials for Rigid and Multilayer Printed Boards.*

Contrary to normal high-speed design practices, the material has a high dielectric constant (Dk), which increases capacitance, and a high dissipation factor (Df), which dampens electromagnetic energy through the relatively high loss of the material.

Embedded capacitance technology has a very thin dielectric layer (0.24–2.0 mil), which provides distributive decoupling capacitance and takes the place of conventional discrete decoupling capacitors over 1 GHz. These ultra-thin laminates replace conventional power and ground planes and have excellent stability of dielectric constant and dielectric loss up to 15 GHz. The thinner layers of ECM also significantly reduce the capacitor mounting inductance.

The embedded capacitor layer can be placed anywhere in the board stackup (including outer layers if desired). Multiple layers can be used to increase capacitance and lower inductance. Placing the embedded capacitor layer closer to the surface (closer to the ICs as in Figure 2) will reduce via inductance and make the capacitance material more effective, especially



Layer No.	Via	Description	Layer Name	Material Type	Dielectric Constant	Dielectric Thickness	Copper Thickness	Trace Clearance	Trace Width	Current (Amps)	Characteristic Impedance (Zo)	Edge Coupled Differential (Zdiff)	Broadside Coupled Differential (Zdbs)	Notes
		Soldermask		Dielectric	3.3	0.5								
1	8	Signal	Top	Conductive			1.4	12	4	0.31	51.19	98.66		Signal/Power
		Prepreg		TU-66P; 11080; RC=63%; (1MHz)	4.5	2.9								Tg=160C; Df=0.01
2		Plane	GND	Conductive			1.4							GND
		Core		3M ECM; C2006; 20nF/in2 (1kHz)	22	0.24								Tg=120C; Df=0.01
3		Plane	VDD	Conductive			1.4							Power
		Prepreg		TU-66P; 7628; RC=45%; (1MHz)	4.9	7.7								Tg=160C; Df=0.01
4		Signal	Signal	Conductive			1.4	18	3.5	0.28	49.79	98.75		
		Core		TU-662; 1-1506; RC=50%; (1MHz)	4.9	6								Tg=160C; Df=0.01
5		Plane	GND	Conductive			1.4							GND
		Prepreg		TU-66P; 2116; RC=62%; (1MHz)	4.6	6.1								Tg=160C; Df=0.01
6		Signal	Inner 6	Conductive			1.4	18	4	0.31	50.2	98.99	69.93	Signal/Power
		Core		TU-662; 2-1080; RC=50%; (1MHz)	4.6	5								Tg=160C; Df=0.01
7		Signal	Inner 7	Conductive			1.4	18	4	0.31	50.2	98.99	69.93	Signal/GND
		Prepreg		TU-66P; 2116; RC=62%; (1MHz)	4.6	6.1								Tg=160C; Df=0.01
8		Plane	GND	Conductive			1.4							GND
		Core		TU-662; 1-1506; RC=50%; (1MHz)	4.9	6								Tg=160C; Df=0.01
9		Signal	Signal	Conductive			1.4	18	3.5	0.28	49.79	98.75		
		Prepreg		TU-66P; 7628; RC=45%; (1MHz)	4.9	7.7								Tg=160C; Df=0.01
10		Plane	VCC	Conductive			1.4							Power
		Core		3M ECM; C2006; 20nF/in2 (1kHz)	22	0.24								Tg=120C; Df=0.01
11		Plane	GND	Conductive			1.4							GND
		Prepreg		TU-66P; 11080; RC=63%; (1MHz)	4.5	2.9								Tg=160C; Df=0.01
12		Signal	Bottom	Conductive			1.4	12	4	0.31	51.19	98.66		Signal/Power

Figure 2: High-speed 12-layer stackup using 3M, ECM of 0.24 mil core thickness.

Table 1: Embedded capacitor materials available in the ICD dielectric materials library

Manufacturer	Material	Description	Thickness (mil)
3M	ECM	Embedded Capacitance Material (ECM)	0.24, 0.47, 0.55
DuPont	Interra HK04	Ultra-thin laminate	0.5, 1.0
Integral Technology	Zeta Bond	High Tg Epoxy Based adhesive film	1.0, 1.5, 2.0
Integral Technology	Zeta Lam SE	Low CTE C-stage dielectric with a Hi Tg	1.0
Integral Technology	Zeta Cap	Hi-performance polymer coated copper	1.0
Oak-Matsui Technology	FaradFlex	Planar capacitor	0.31,0.47,0.63,0.94
Samina	ZBC1000	Buried Cap, hi-performance decoupling	1.0
Samina	ZBC2000	Buried Cap, hi-performance decoupling	2.0

at high frequencies. If more than one embedded capacitance layer is used, they should be distributed so there is a balanced stackup and board warping is kept to a minimum. This also provides decoupling of ICs on the bottom side of the PCB.

The ZBC-2000 laminate uses a single ply of either 106 or 6060 style prepreg, yielding a dielectric thickness after lamination of 2 mils as measured by cross-sectioning. Similarly, ZBC-1000 results in a 1-mil dielectric distributed capacitance material. FaradFlex and Interra buried capacitance products utilize a durable resin system for non-reinforced dielectrics for 1 mil thickness and below. This eliminates the skew associated with the fiber-weave effect in standard materials. Also, with a product range of up to 20 nF per square inch in capacitance density, 3M ECM is the highest capacitance density embedded capacitance material on the market.

These ultra-thin laminates allow a significant layer count reduction in PCBs with better signal performance. With a high withstanding voltage, these glass-free films change the design rules for via diameter and trace width, while still conforming to the manufacturing needs of the fab. Three traces between vias, at a 0.4 mm pitch, are possible and very manufacturable, according to Integral Technology.

It is a common belief that solid power and ground planes act as large, perfect, lumped element capacitors. However, they actually encompass a distributed system of surprising complexity. The distinction between a lumped element and a distributed system involves the relationship between the time delay of the system and the rise time of the signals.

For instance, for a PCB of six square inches, the signals entrapped between the VCC and GND planes create a standing wave, resonating as they reflect from side-to-side, and have a delay time of about 1 ns. If the rise-time of the signal is 5 ns, the lumped condition is satisfied. However, with a much faster rise-time or if the plane is very small (typically one-inch square), then the driver perceives the VCC and GND structure as a distributed object with significant delay. This often occurs on mixed signal/power layers.

This delay causes two issues:

1. During the rising and falling edge, only the portion of the planes and decoupling capacitors located within the close vicinity of the driver can react before the edge has vanished. This frequently results in the noise spike being larger than anticipated.

2. The residual PDN noise from the first event reflects in the cavity (which resembles an unterminated transmission line) a couple of nanoseconds later, back to the driver. If at that precise moment, the driver switches a second time, both pulses (first and second) are superimposed. If the phases are added and the driver has a repetitive pulse (as clocks do), the reflected pulse may build significantly into a standing wave.

One could avoid this potential failure by comparing the round-trip delay across the plane in question to the clock period. If it is close, then an adjustment in the plane size may be an appropriate solution. This may not eliminate all plane resonances but can serve to shift the resonances to other frequencies. Also, adding stitching vias or terminating RC networks in appropriate locations can reduce the extent to which the signal energy spreads through the plane cavity and raises the frequency of structural resonances.

Replacing conventional power/ground planes with an embedded capacitance layer allows for tighter component density, reduced via count, and thus increased signal routing channels. ECMs provide higher capacitance in a PDN, resulting in lower AC impedance and greater damping for power bus ripple. This leads to less intense power plane cavity resonances at gigahertz frequencies due to the material's higher dielectric constant and loss tangent. This lossy property is what makes these materials so useful for power integrity, even when there are insufficient decoupling capacitors. It dampens signal propagation beginning at a lower frequency cut-off and can reduce the signal level if the core voltage is low and/or the routing channel is long.

Key Points

- Embedded capacitance material can improve power integrity dramatically by reducing AC impedance and generally enhancing the performance of the product.
- Decoupling capacitors are only effective up to a few hundred megahertz. Above that, only on-die capacitors or planar capacitance can reduce the impedance significantly due to their low inductance.
- ECM comprises copper-clad laminates with very thin dielectric thickness and high dielectric constant and loss. These materials can replace standard power and ground planes.
- The high Dk increases capacitance and the high Df dampens electromagnetic energy through the relatively high loss of the material.
- These ultra-thin laminates replace conventional power and ground planes.
- Placing the embedded capacitor layer closer to the surface of the stackup will reduce via inductance and make the capacitance material more effective.
- The distinction between a lumped element and a distributed system involves the relationship between the time delay of the system and the rise time of the signals.
- If the plane is very small, then the driver perceives the VCC and GND structure as a distributed object with significant delay.
- If the phases add and the driver has a repetitive pulse (as clocks do), the reflected pulse may build significantly into a standing wave.

Resources

1. Beyond Design by Barry Olney: "The 10 Fundamental Rules of High-Speed PCB Design Part 3," "Plane Crazy, Part 2."

2. "Fabrication of Embedded Capacitance Printed Circuit Boards," by Joel S. Peiffer, 3M.

3. "Embedded Capacitance Material Properties," by Cadence PCB Solutions.

Barry Olney is managing director of In-Circuit Design Pty Ltd (iCD), Australia, a PCB design service bureau that specializes in board-level simulation. The company developed the iCD Design Integrity software incorporating the iCD Stackup, PDN, and CPW Planner. The software can be downloaded at www.icd.com.au. To read past columns, click here.