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The Dumping Ground

by Barry Olney

IN-CIRCUIT DESIGN PTY LTD AUSTRALIA

A ground plane in a PCB assembly is a layer of copper that appears to most signals as an infinite ground potential. This helps reduce noise and helps ensure that all integrated circuits within a system compare different signals' voltages to the same reference potential. Ground planes can also be placed on adjacent layers to power planes, creating a large parallel plate capacitor that helps filter the power supply. It also serves to make the circuit design easier, allowing the designer to ground anything without having to run multiple tracks; the component needing grounding is routed directly to the ground plane on another layer.¹

Hmm! Well, actually, that may be the case with DC or very low frequency and analog circuits, but certainly not when we are talking high-speed design.

In a DC circuit, the return current takes the path of least resistance—sort of like pouring a bucket of water on the ground. The water takes the path of least resistance and follows the troughs to the lowest point. However, at high speed (> 30 MHz) the return current takes the path of least inductance, which just happens to be the reference plane (either ground or power) directly below the trace.

The ground plane is not a dumping ground for unwanted signal returns. Figure 1 is an example of what the ground plane would

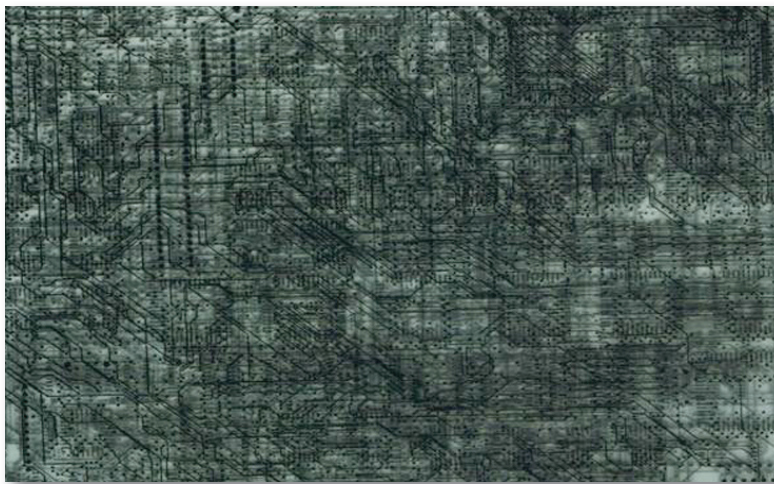


Figure 1. Ground is not a sheet of copper.

SUMMARY

By definition, a ground plane in a PCB assembly is a layer of copper that appears to most signals as an infinite ground potential. This month, we discuss best practices for selecting reference planes and routing pairs for high-speed designs on multilayer boards.

look like if one reference plane were used for a number of signal layers.

The return currents follow the path of least inductance with the streams of electrons crossing over each other. Although this is probably immeasurable, one would

assume that there would be some sort of detrimental interaction (crosstalk) between these streams. This is why each signal layer should have a dedicated reference plane.

One point that always amazes me: designers generally take great care to ensure that matched length signals are routed exactly to length from the driver to the DRR2 device pin, but take no care of the return path of the signal. Current flow is a 'round trip.' If it takes one signal longer for the return current to get back to the driver (around a gap in the plane for instance) then there will be skew between the critical timing signals.

When you plan your stackup, be aware of which plane(s) (either power or ground) will be the return path for your critical signals and make sure there is an unobstructed return path. The best way to think of this is to imagine routing a return trace adjacent to each signal trace on the reference plane—where is the best place for the current to flow and is it unobstructed? The reference plane adjacent to each signal layer allows the return current to

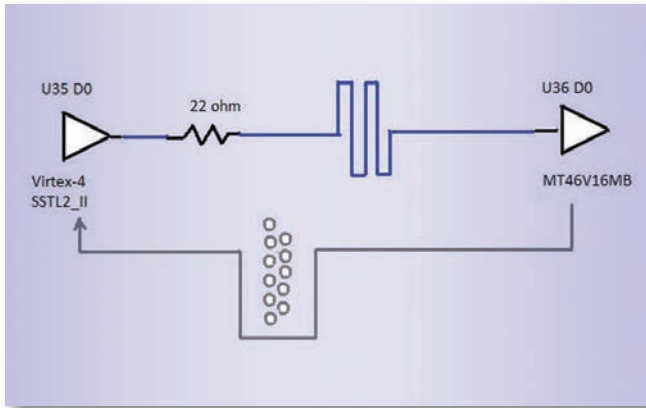


Figure 2. The return current for a data signal diverts around the connector antipads in the plane.

flow as closely as possible to the signal trace, reducing inductance and loop area.

The ideal high-speed stackup is illustrated in Figure 4. This eight-layer stackup is commonly used for DDR2 & DDR3 designs as each signal layer has a reference plane on both sides, thus avoiding crosstalk from adjacent signal layers and providing a clear return path for the current. This stackup has been built with the ICD Stackup Planner (download from www.icd.com.au).

Layer pairs for routing the memory are 1 & 3 (data lanes & strobes) and 1 & 6 (address bus & clocks), using GND for both reference planes. 90 ohm differential USB signals can be routed on layer 3. Single-ended 50 ohm signals on any layer and differential 100 ohm signals on any other layer.

If possible, we should use the one reference plane for the return path. In this case, we have used GND, but the return path can be any reference plane ground or power. Choosing layer 2 for the reference plane allows the return current to initially follow the signal path on the top surface of the GND plane, then crossing over to the bottom surface through the via antipad so it is as close as possible to the signal path. This is called the ‘skin effect.’ At high frequencies, current doesn’t flow evenly through the entire cross section of the copper plane but is more concentrated at the surface. Because of the skin effect, at high frequencies, the current can’t pass through the copper plane (the plane acts more like a hollow conductor) and has to go from top to bottom surface through the via antipad.

An interesting scenario is if we swap plane layers 4 & 5 (VCC & GND). In this case, VCC would be used for the reference plane in the drawing to the right. So how will the return current get back to the driver from layer 5? It’s a shame that electrons can’t fly. The current will have to go to the nearest DCAP between VCC and GND to jump layers. If there is no DCAP nearby, this may be as far away as the power supply, creating a huge loop area and hence radiation (EMI). Therefore, it is important to place a DCAP close to every via to aid the return signal. That reminds me of another one of my wise sayings: “Wherever there is room, place another DCAP.” You can never have too many.

ICD STACKUP PLANNER – www.icd.com.au 7/14/2011											Total Board Thickness: 61.2	
UNITS: MIL												
Layer	Material	Dielectric		Copper	Trace		Current	Impedance	Edge Coupled	Broadside Coupled	Description	
Number	Name	Type	Constant	Thickness	Thickness	Clearance	Width	(Amps)	Characteristic(Zo)	Differential(Zdiff)	Differential(Zdbs)	
1	Top	Dielectric	3.3	0.5								Soldermask
		Conductive			1.4	8	4	0.31	53.53	99.99		Signal
		Dielectric	4.3	3								Prepreg
2	GND	Conductive			1.4							Plane
		Dielectric	4.3	8								Core
3	Inner 3	Conductive			1.4	12	5	0.37	51.96	90.66		Signal
		Dielectric	4.3	8								Prepreg
4	VDD	Conductive			1.4							Plane
		Dielectric	4.3	12								Core
5	GND	Conductive			1.4							Plane
		Dielectric	4.3	8								Prepreg
6	Inner 6	Conductive			1.4	12	4	0.31	56.4	98.4		Signal
		Dielectric	4.3	8								Core
7	VCC	Conductive			1.4							Plane
		Dielectric	4.3	3								Prepreg
8	Bottom	Conductive			1.4	8	4	0.31	53.53	99.99		Signal
		Dielectric	3.3	0.5								Soldermask

Figure 3. Ideal 8 layer stackup.

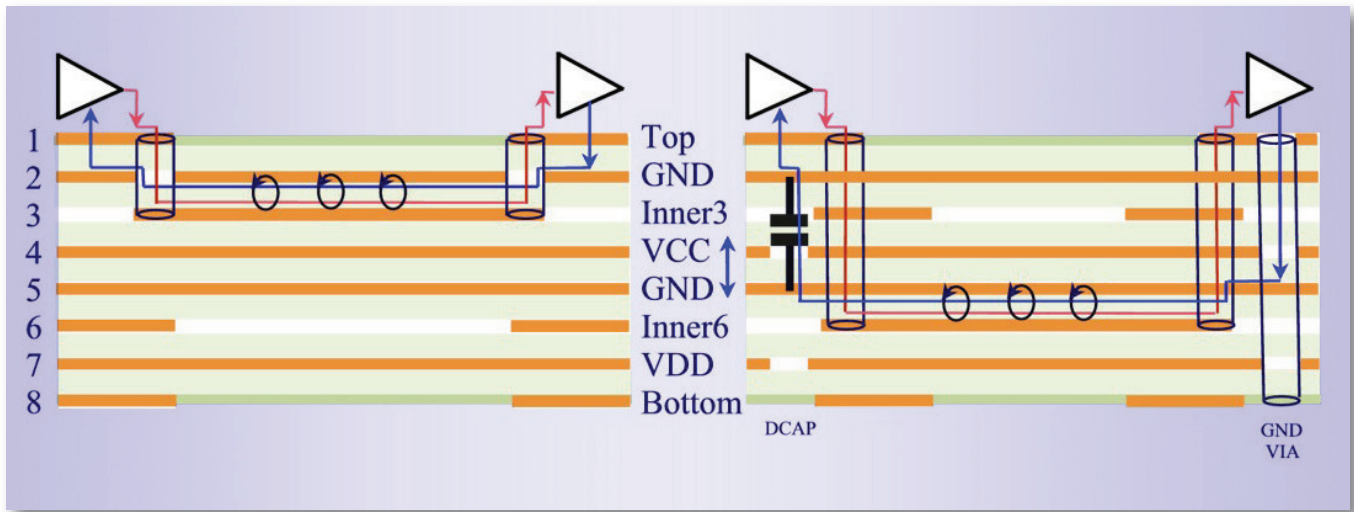


Figure 4. Signal and return paths for routing pairs.

In order to change reference planes:

- If there are multiple ground planes, place a stitching via as close as possible to each signal via.
- If power planes are also used as the reference plane, place DCAPs as close as possible to each signal via.

Also, please keep in mind that high-speed signals should not be routed on the outer layers. Embedding the signals between the planes (on layers 3 & 6) reduces the radiation by at least 10 dB. So, fan out from the driver and drop to the internal signal layer routing up to the load through a short stub.

In conclusion, the PCB designer must route the signal trace and mentally route the return path in order to keep flight times tight, crosstalk low and radiation (EMI) to a minimum. The best way to think of this is to imagine routing a return trace adjacent to each signal trace on the reference plane—where is the best place for the current to flow and is it unobstructed? **PCB**

References:

1. Wikipedia
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3. Advance Design for SMT – Barry Olney
4. Design for EMC – Barry Olney
5. Electromagnetic Compatibility Engineering – H. Ott
6. High Speed Design – H. Johnson
7. The ICD Stackup Planner can be downloaded from www.icd.com.au



Barry Olney is Managing Director of In-Circuit Design Pty Ltd. (ICD), Australia, a PCB Design Service Bureau and Board Level Simulation Specialist. Among others through the years, ICD was awarded “Top 2005 Asian Distributor Marketing and “Top 2005 Worldwide Distributor Marketing by Mentor Graphics, Board System Division. For more information, contact Barry Olney at +61 4123 14441 or email at b.olney@icd.com.au.

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