

Design for Profit

by Barry Olney | In-Circuit Design Pty Ltd | Australia

Completing the project on time and within budget minimizes costs.
Reducing the design cycle generates higher profits due to shorter time to market which in turn extends the product life cycle.

Design for Profit (DfP) typically eliminates inefficiency in the traditional design process. Reducing part count and simplifying assembly results in lower cost, better quality and higher profits – all delivered before manufacture begins. DfP also encompasses Design for Manufacturability (DfM). DfM is the practice of designing board products that can be produced in a cost effective manner using existing manufacturing processes and equipment.

DfP is gaining more recognition as it becomes clear that the cost reduction of printed circuit assemblies cannot be controlled by manufacturing engineers alone. The PCB Designer now plays a critical role in cost reduction.

However, as we grow as PCB Designers our focus changes from basic considerations to more complex system level initiatives. PCB Designers require attention to detail, an artistic talent, the capacity to accept change and the ability to deliver on time under constant pressure. Also, the requirements for a PCB design can vary considerable from one design to another. However, attributes that increase profit are self taught and require time to develop.



Fig 1. Three levels of the PCB Designer – which level are you at?

There are three levels of the PCB Designer:

1. PCB Schematic and Layout Designer

I guess this is where we all first started many years ago. His focus is on a single event – the current product and the ability to design at the technology level involved in the project. He uses features within the tools to enhance the design. He takes price of components into account in order to reduce the total price of the build. He absorbs information such as design rules and best practices to constantly improve his skills.

At this level of knowledge, the enhancements that can be made to the design include basic setup costs:

- Standard design rules
 - Consistency encourages good design practice and streamlines design
- Technology – trace width/clearance, via type and complexity
 - 4/4 technology and through hole vias are cheaper than 3/3 and microvias
- Layer count
 - The fewer the layers and the fewer number of core materials the cheaper the fabrication
- Hole size
 - Reducing via holes below 8 mils will incur more cost
- Copper thickness
 - Thinner copper is cheaper but there are trade-offs between cost and reliability
- Stencil Apertures
 - Correct apertures improves production yields

2. PCB Specialist

This guy manages other PCB Designers, or runs his own business, and has years of experience. He has a business agenda and focuses on the overall costs of development and manufacture and the benefits he can deliver from a strategic point.

The PCB Specialist's interest lies in the development, fabrication, assembly and testing processes. He improves the process by reusing existing design snippets, standardizing library components, to reduce stock holding costs, panelizes boards for mass production and schedules delivery times to work in with the requirements of the testing and manufacturing sectors.

The PCB Specialist reduces overall cost by employing the following:

- Design reuse
 - Reuses existing snippets that saves time and adds confidence
- Panelization and standard form factor
 - Standardizes jigs to reduce production, assembly and testing costs
- Test fixture reuse
 - Minimizes the movement of test points during revisions
- Dielectric materials
 - Selects correct materials for performance and price
- Symmetrical stackup
 - Ensures symmetry which reduces wrapping during both fabrication and reflow
- Standardization of library components and values
 - Reduces stock holding costs and assembly setup time
- Component packaging
 - Selects packages that produce higher yields and reduce size
- Volume production and off-shore manufacture
 - Higher volume – the less the cost
- Delivery time and premiums
 - Plans the delivery to scheduled production

3. PCB Design Advisor

The PCB Design Advisor is a design consultant who advises others on the best possible outcome for the project. He works at the executive level to add value and profit to the solution. He focuses on the overall product reliability, system integrity and the solution space from concept to final market deployment. His insight into development is profit making at the competitive level. He controls time to market, competitive advantage and the market window.

The PCB Design Advisor leverages the following:

- Operating Environment
Considers the entire product environment, heat flow, EMI etc
- Reliability
Performs signal integrity and timing analysis to improve product reliability
- System integrity
Analyses the stackup, PDN, signal integrity, crosstalk and EMI
- Competitive advantage
Ensures ease of use, speed and functionality
- Time to market
Reduces development time
- Market window
Ensures the product is in the market longer to increase profits

Allow me to put on my marketing hat for a moment. If we are designing a consumer, computer based, product then the market window (time to sell the product) is probably about one year. Let's say that the design failed to work properly – or at all – on the first build. The next iteration, of the board, will typically take 3 months, delaying the time to market by one quarter of its life cycle. If the Sales department expects to make \$10m on this product, during its projected life, then the profit is reduced by \$2.5m (not to mention the re-design costs). This is where the PCB Design Advisor comes in.

Having the project completed on time and within budget, means that costs are cut by reducing the design cycle and generating higher profits due to shorter time to market and an extended product life cycle.

Price and cost are two different things. The price paid to develop the product is an investment – not a cost. But, it is important to remember what it costs if things go wrong. For each day, week or month that the project is delayed, costs not only in additional labor but also in lost opportunity in getting you product to market.

In a previous column, [Intro to Board-Level Simulation and the PCB Design Process](#), I mentioned that the cost of development is dramatically reduced if simulation is employed during the design cycle. If changes are made late in the design process, then it takes more time, people, material and therefore money to complete the project. The advantage of board level simulation is that it identifies issues EARLY in the design process and rectifies them before they become a major problem.

As can be seen from the graph in Figure 2, design changes that occur in the conceptual stage cost nothing; during the design stage requires just a little extra time; during the test stage means that you have to go back one stage and re-design and during production, or worse still - in the field, can cost millions to fix and possibly damage the company's reputation.

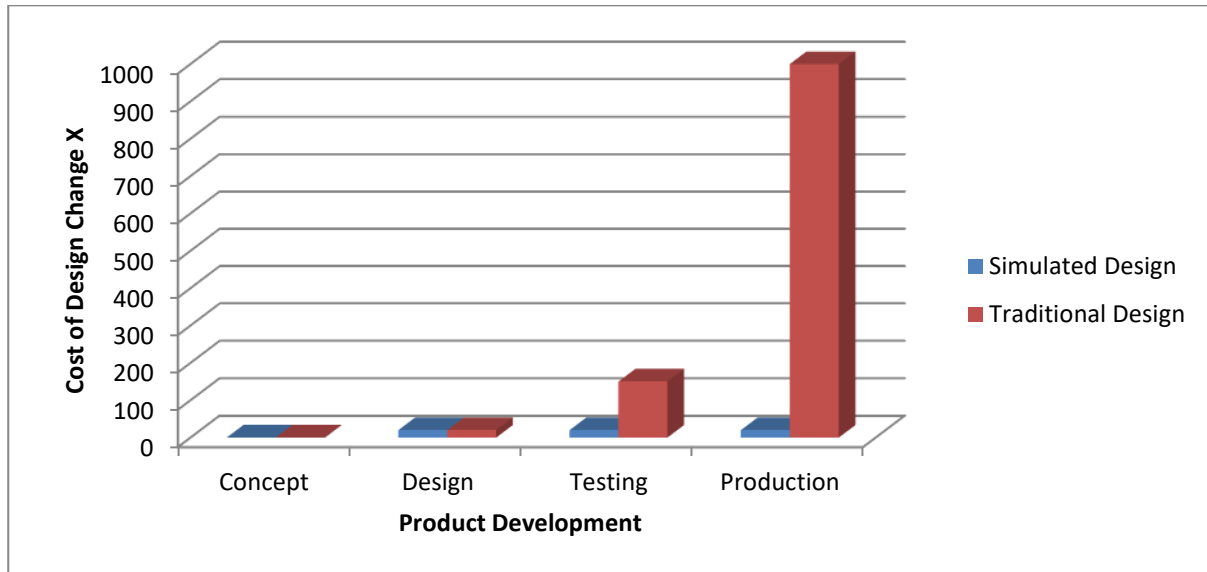


Fig 2. The estimated cost of design change during product development

However, using board level simulation cuts costs: a pre-layout simulation identifies issues in the conceptual stage so that they can easily be avoided. And, the post-layout simulation catches the issues during the design process eliminating the potentially disastrous final stage changes. Of course, we also need to keep our eye on the ball during the entire design process catching any small issue before it becomes a major problem.

The PCB Design Advisor adds value and profit at many levels by performing reliability and system integrity checks before and during the design process:

1. Plans the board stackup from the beginning, ensuring that both single-ended and differential impedances conform to the technology requirements. And, ensures that the selected materials are available from the chosen fabrication shop — this step is regularly missed.
2. Ensures that there is a stable power delivery system. Power Distribution Network (PDN) analysis, of all supplies, ensures that the AC impedance is low over the entire spectrum. The PDN design is also a very important part of the conceptual design process that is often overlooked.
3. Performs a pre-layout simulation to calculate placement and routing constraints. Pre-layout simulation allows the designer to predict and eliminate signal integrity, crosstalk and EMC issues early in the design process. This is the most cost effective way to design a board with fewer iterations rather than starting with the post-layout simulation.
4. Ensures that the correct Design Rules – based on simulation – are set-up prior to placement and routing. Design rules should be defined and attached to critical nets in the schematic. This allows the Engineer to transfer his desired intent, with regard to placement and routing, to the PCB Designer without the information being lost in the process.
5. Performs a post-layout simulation to ensure the timing is to spec. Simulates trouble spots identified by the batch analysis in order to further resolve the issues with greater accuracy.

You are not just a PCB Designer – you need to add value to each design and continue to increase profit for your employer. A good PCB Designer prevents rather than reacts to problems.

Points to remember:

- The PCB Designer plays a critical role in cost reduction
- There are three levels of PCB Designer: PCB Layout Designer, PCB Specialist and PCB Design Advisor.
- Having the project completed on time and within budget, means that costs are cut by reducing the design cycle and generating higher profits due to shorter time to market and an extended product life cycle.
- The cost of development is dramatically reduced if simulation is employed during the design cycle.
- The PCB Design Advisor adds value and profit, at many levels, by performing reliability and system integrity checks before and during the design process.
- A good PCB Designer prevents rather than reacts to problems.

References:

Advanced Design for SMT – Barry Olney

[Intro to Board-Level Simulation and the PCB Design Process](#) – Barry Olney

[Board Level Simulation and the Design Process: Plan B: Post Layout Simulation](#) – Barry Olney

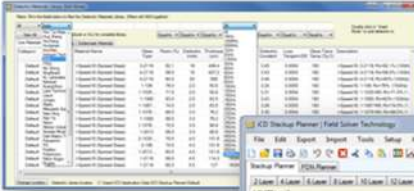
The ICD Stackup and PDN Planner can be downloaded from www.icd.com.au

Bio - Barry Olney is Managing Director of In-Circuit Design Pty Ltd (ICD), Australia. The company developed the ICD Stackup Planner and ICD PDN Planner software, is a PCB Design Service Bureau and specializes in board level simulation.


iCD Design Integrity

Incorporates the iCD Stackup, PDN and CPW Planner software. Offers PCB Designers unprecedented simulation speed, ease of use and accuracy at an affordable price

Dielectric Materials Library
31,250 Rigid & Flex Materials to 100GHz




iCD Stackup Planner
Field Solver Accuracy, Characteristic Impedance, Edge & Broadside Coupled Differential Impedance

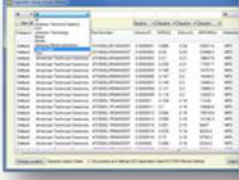


Layer	Material Type	Dielectric Constant	Dielectric Loss	Copper Thickness	Trace Width	Trace Spacing	Current (Amps)
1	PSR-4000 HF Flex (C442 HF LP)	3.5	0.005	2.2	12	6	0.58
2	ST5485 100% Rm 96% (10GHz)	3.87	2.9	1.4			
3	ST5485 1-1802 Rm 42% (10GHz)	4.4	5	1.4			
4	ST5485 2118 Rm 96% (10GHz)	4.14	4.8	1.4	12	6	0.42
5	ST5485 1-1802 Rm 42% (10GHz)	4.4	5	1.4			
6	ST5485 106 Rm 76% (10GHz)	3.74	2.3	1.4			
7	ST5485 1-1802 Rm 42% (10GHz)	4.4	5	1.4			
8	ST5485 2118 Rm 96% (10GHz)	4.14	4.8	1.4	12	6	0.42
9	ST5485 1-1802 Rm 42% (10GHz)	4.4	5	1.4			
10	ST5485 100% Rm 96% (10GHz)	3.87	2.9	1.4			
11	PSR-4000 HF Flex (C442 HF LP)	3.5	0.005	2.2	12	6	0.58

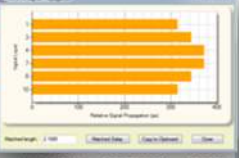
iCD CPW Planner
Model single and dual (differential) Coplanar Waveguides, with and without reference planes, plus a dual Coplanar Strip (CPS).



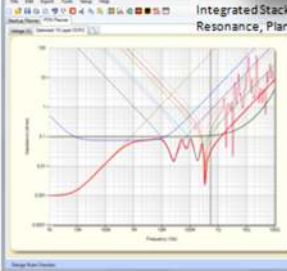
Extensive Capacitor Library
5,650 Decaps Derived from SPICE Models



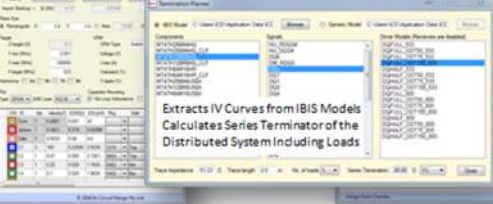
Matched Delay Optimization
Relative Signal Layer Propagation
Ideal DDRx Trace Delay Matching



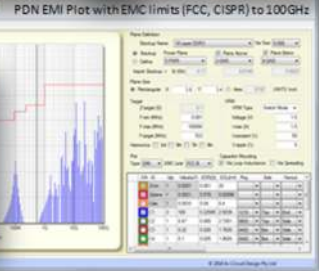
iCD PDN Planner
AC Impedance Analysis & Plane Resonance



iCD Termination Planner
Extracts IV Curves from IBIS Models
Calculates Series Terminator of the Distributed System Including Loads



PDN EMI Plot with EMC limits (FCC, CISPR) to 100GHz



© 2013 In-Circuit Design Pty Ltd