

Balancing Trade-offs for Optimal PCB Design

Beyond Design

Feature Column by Barry Olney, IN-CIRCUIT DESIGN PTY LTD / AUSTRALIA

The field of PCB design is evolving rapidly, which creates both opportunities and demands for new and experienced designers. PCB designers must deal with various issues in finding the right balance between the form factor, functionality, and power requirements of their boards while ensuring that the stackup, placement, and routing are completed to guarantee stringent signal and power quality. Advanced tools and skills are needed to create compact, flexible, high-performance, and low-power PCBs with faster turnaround times. There is also a trend to collaborate with other designers and manufacturers in a team environment through cloud-based platforms to ensure that the designs are reliable and manufacturable.

As multilayer PCBs become more complex, PCB designers face the challenge of cramming more components and connections onto a limited board area without compromising performance or quality. Increasing the number of signal layers can help to accommodate more signal routing and reduce crosstalk, but there are inevitable bottlenecks in the breakout of high pin-count devices. The use of high-density interconnects, blind and buried vias, and via-in-pad techniques also help to alleviate these issues.

Ball grid array (BGA) packages come in a variety of pitches and sizes. As device complexity increases and OEMs continue their drive toward smaller components, ball pitches

**FORM
FACTOR**

FUNCTIONALITY

**POWER
REQUIREMENT**

Table 1: Typical feature sizes for BGAs. (Source: PCBLibraries)

BGA Pin Pitch	BGA Ball Dia	BGA Land Size	Land Hole Size	Plane Clearance	Trace Width	Trace/Trace Space	Trace/Via Space	Trace/Land Space	Route Grid	Part Place Grid
0.4	0.25	0.25	0.125	0.35	0.05	0.05	0.05	0.05	0.05	0.5
0.5	0.3	0.275	0.15	0.425	0.075	0.075	0.075	0.075	0.05	0.5
0.65	0.4	0.4	0.15	0.5	0.1	0.1	0.1	0.075	0.05	1
0.65	0.4	0.425	0.2	0.575	0.075	0.075	0.075	0.075	0.05	1

of 0.5 mm and lower are becoming more popular. Today, there are 0.4-mm pitch BGAs in virtually every smartphone, and 0.3-mm ultra-fine pitch BGAs are the next generation. The next step is to increase functionality within the same package. Early adopters are venturing into the 0.3-mm pitch devices. However, there are currently no formal IPC design guidelines or layout rules specifically tailored to supporting 0.3-mm pitch devices. As a result, many PCB designers largely rely on traditional 0.5-mm pitch design guidelines and layout rules to develop new 0.3-mm pitch device-based designs. For instance, the current design guidelines allow the use of a solder-ball-joint pad with a diameter of 20% less than the diameter of a BGA/CSP solder ball.

Table 1 gives an example of the required feature sizes for BGAs. This enables us to determine the signal layer count required to breakout from fine-pitch BGAs. The minimum number of signal routing layers required to route a particular design can be estimated once the location of the signals on the BGA is known.

- The first two rows/columns will route on one signal layer
- The second two rows/columns will route on a second signal layer

Plus, an additional signal layer is generally required for every row of signal balls past four rows.

This assumes that all balls are routed because their signals are needed for connectivity. But if some balls are no-connects, then those corresponding ball escape lanes are free for other

signals. In this regard, fewer layers may suffice if the required signals have enough viable routing lanes. Blind microvias and vias-in-pad are normally required for the breakout of 0.5-mm pitch or less.

Accommodating the high number of individual power supplies to the BGA is also an issue. One can generally place three to four power pours on each power layer depending on the BGA pinout. So, four power layers typically are required for 10 supplies plus ground. This could be reduced if some of the power pours are combined with signals on a mixed layer.

As the data rate increases, the bandwidth required for data transmission also increases, which poses challenges for PCB design such as signal integrity, crosstalk, impedance matching, and electromagnetic interference. The PCB designer must also balance the layer count vs. manufacturing complexity. Signal integrity requirements may also impact this decision if, for instance, parallel trace segments are over 12 mm in length with a 200 ps rise time.

PCB design is a complex and challenging task that requires designers to consider various aspects that influence the performance and quality of the PCB. Among these aspects, signal integrity, power integrity, thermal management, and electromagnetic compatibility are crucial for ensuring the functionality and reliability of the PCB. PCB designers need to acquire more knowledge and skills to analyze and optimize these aspects of PCB design using appropriate principles, methods and tools.

radiate to create more EMI. Apart from the issues of EMI, signal integrity, and crosstalk, this noise can cause intermittent operation of the product due to timing glitches and interference, dramatically reducing the reliability of the product. Excessive ringing can also lead to power integrity issues.

Flight time delay and skew are the key pillars in high-speed PCB design signal integrity. One of the driving factors for flight time and skew performance is the placement of components. In the classic high-speed design flow, timing specifications simulation results are compared to determine placement and routing constraints. Given a length constraint, a designer can control signal integrity by controlling the PCB trace topology of the various parts of an interface. Included in this topology are any terminations. Figure 2 shows an eye diagram of a signal with jitter and ringing due to poor termination.

The integrity of the PCB stackup and the PDN are the basis for a stable product. Multi-

layer PCB design is becoming more complex and less forgiving—it's not just about signal integrity, crosstalk, and EMI. The substrate and the power delivery system are extremely critical and if they should fail then the whole system can go down or, in the worst case, may just work intermittently.

Today's high-performance processors employ low DC voltages with high transient currents and high clock frequencies to minimize power consumption and hence the amount of heat dissipated. A typical high-speed design contains 10 or more individual power supplies. And unfortunately, the lower core voltages, higher currents, and faster edge rates all impact the power distribution network (PDN) design, as well as signal integrity.

Ideally, the effective impedance of the PDN should be kept below the target impedance up to the maximum required bandwidth. However, if the impedance is too far below the target, then this implies that the PDN has been overdesigned which unnecessarily increases

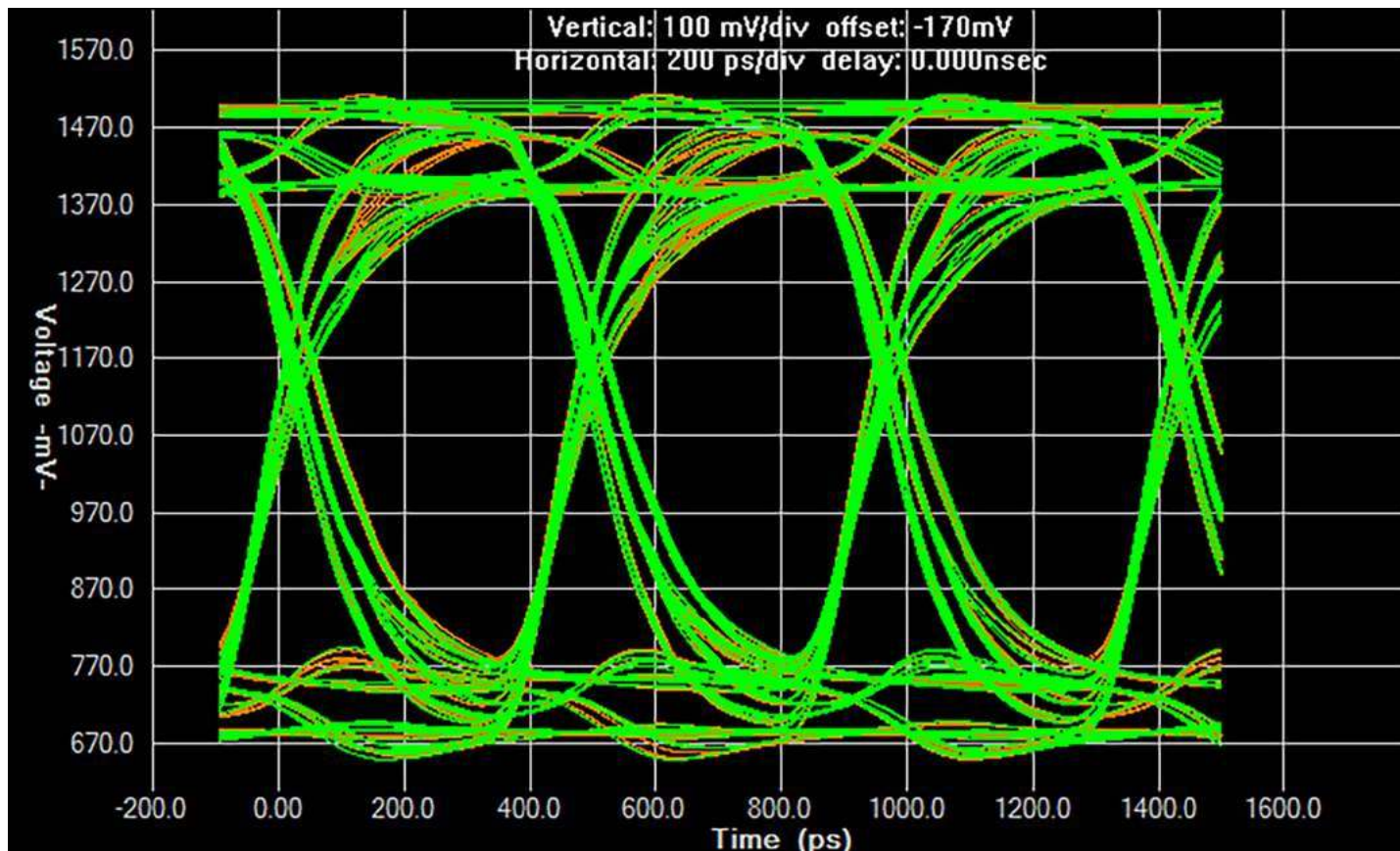


Figure 2: Eye diagram of a signal with poor termination.

costs with little added benefit. If your company intends to build hundreds of thousands of assemblies, then the potential cost saving can be quite significant. Analyzing the PDN ensures the best performance at the most cost-effective price.

Many competent PCB designers will retire within the next few years leaving a void in the knowledge base. This creates a shortage of skilled and experienced PCB designers, increases the demand for new and young PCB designers, and allows for more opportunities for collaboration and innovation among PCB designers. However, the lack of manufacturing knowledge of the upcoming designers can cause design errors and failures, increase the design time and cost, and reduce the manufacturability and yield of the product.

Experience is the best teacher of all. PCB designers need to have more knowledge and skills to design PCBs that have high signal integrity, power integrity, thermal performance, and electromagnetic compatibility. PCB designers must understand the principles, methods, and tools for analyzing and optimizing all aspects of PCB design.

Key Points

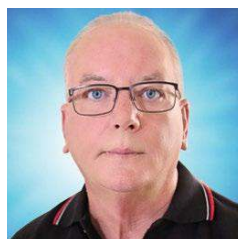
- PCB designers must deal with various issues in finding the right balance between the form factor, functionality, and power requirements of their boards.
- BGA pitches of 0.5 mm and lower are becoming more popular.
- 0.3-mm ultra-fine pitch BGAs and increased functionality within the same package are the next generation.
- Currently there are no formal IPC design guidelines or layout rules specifically tailored to supporting 0.3-mm pitch devices.
- Blind microvias and vias-in-pad are normally required for the breakout of 0.5 mm pitch or less.
- Accommodating the high number of individual power supplies to the BGA is also an issue.

- The increased data rates also require more complex modulation schemes for data encoding, such as non-return-to-zero (NRZ) to pulse amplitude modulation 4-level (PAM4) encoding.
- The impedance should be simulated by a field solver to obtain accurate values of impedance for each signal layer of the substrate.
- Flight time delay and skew are the key pillars in high-speed PCB design signal integrity.
- The integrity of the PCB stackup and the PDN are the basis for a stable product.
- The lower core voltages of today's processors require higher currents and faster edge rates.
- The effective impedance of the PDN should be kept below the target impedance up to the maximum required bandwidth.
- If the impedance is too far below the target, then this implies that the PDN has been overdesigned which unnecessarily increases costs with little added benefit.

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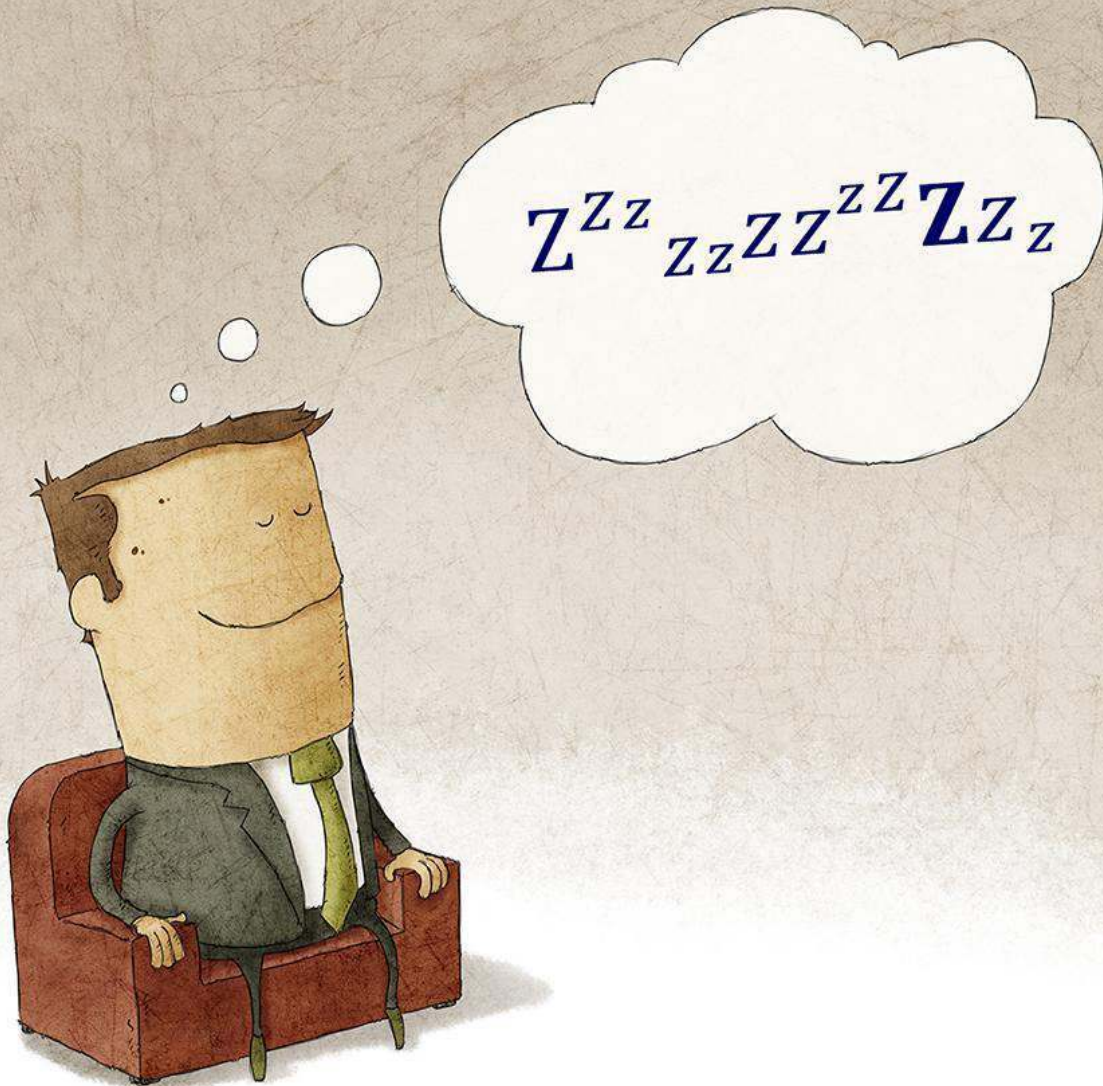
Resources

- Beyond Design by Barry Olney: "Fly-over Technology: When It All Gets Too Fast," "Signal Integrity (Parts 1 & 3)," "The Target Impedance Approach to PDN Design."
- AM57xx BGA PCB Design, Texas Instruments.
- "Metric Pitch BGA and Micro BGA Routing Solutions" by Tom Hausherr.



Barry Olney is managing director of In-Circuit Design Pty Ltd (iCD), Australia, a PCB design service bureau that specializes in board-level simulation. The company developed the iCD Design Integrity software incorporating the iCD Stackup, PDN, and CPW Planner. The software can be downloaded at www.icd.com.au. To read past columns, [click here](#).

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Did you know that two seemingly unrelated concepts are the foundation of a product's performance and reliability?

- Transmission line impedance and
- Power Distribution Network impedance

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– Barry Olney

