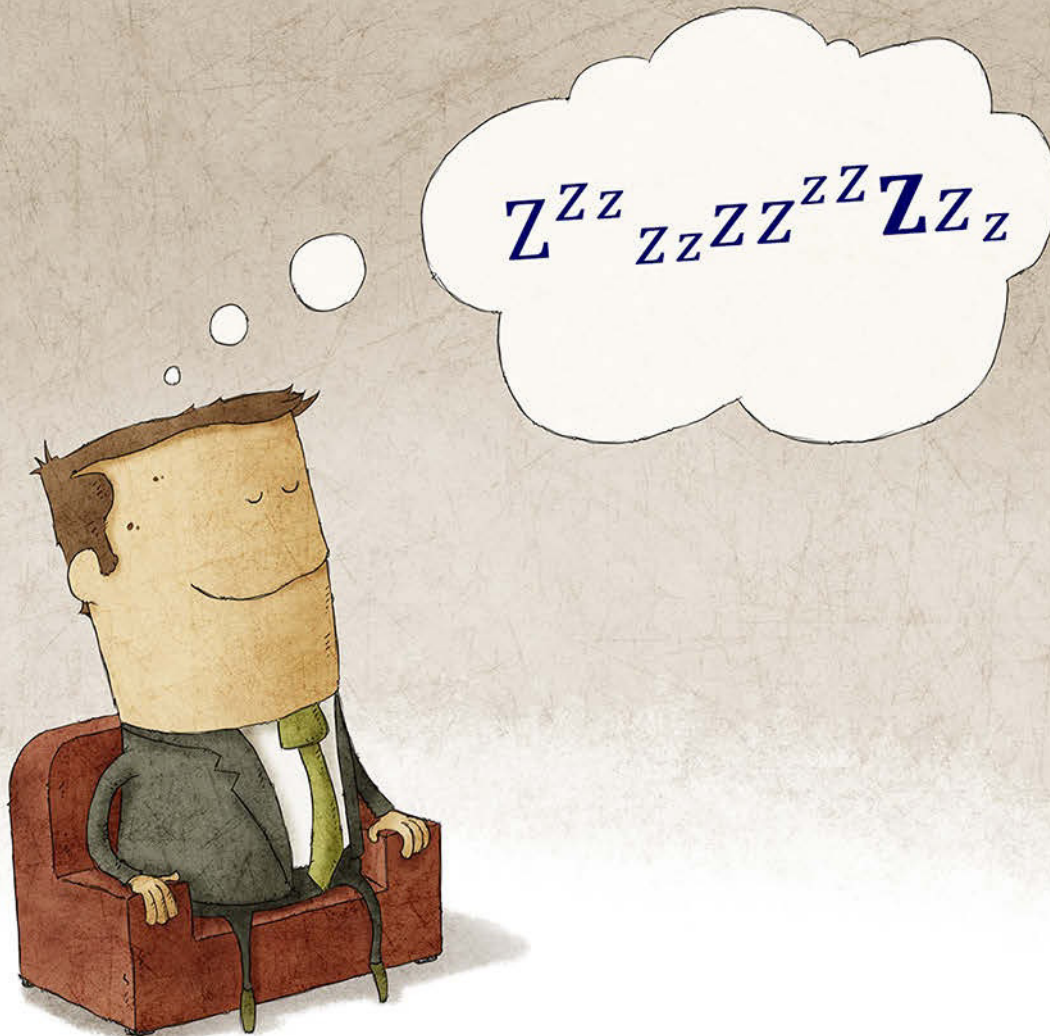


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High-speed PCB Design Constraints

Beyond Design

Feature Column by Barry Olney, IN-CIRCUIT DESIGN PTY LTD / AUSTRALIA

Digital design has entered a new realm. Modern high-speed design (HSD) not only requires the designer to continuously break new ground on a technical level but also requires the designer to account for significantly more variables associated with higher frequencies, faster transition times, and higher bandwidths. Ignoring signal and power integrity and electromagnetic compatibility invites schedule delays and increases development costs and the possibility of never succeeding to build a functional product, which is a career-limiting strategy.

The key methodology is to understand the underlying high-speed design issues and then translate these into corresponding design con-

straints that will be adhered to during the entire design process. It is best to develop these high-speed design constraints based on pre-layout simulation (Figure 1).

We had a few critical nets to manage in the past, but now, it seems that a significant number of interconnects are critical. Also, each design requires a specific set of constraints based on the technologies used. Sure, we can port basic design rules for trace width, clearance, etc., from a previous design to the next, but individual constraints still need to be established. Constraint reuse is also limited by net and group naming conventions. If you are consistent, then porting is much easier.

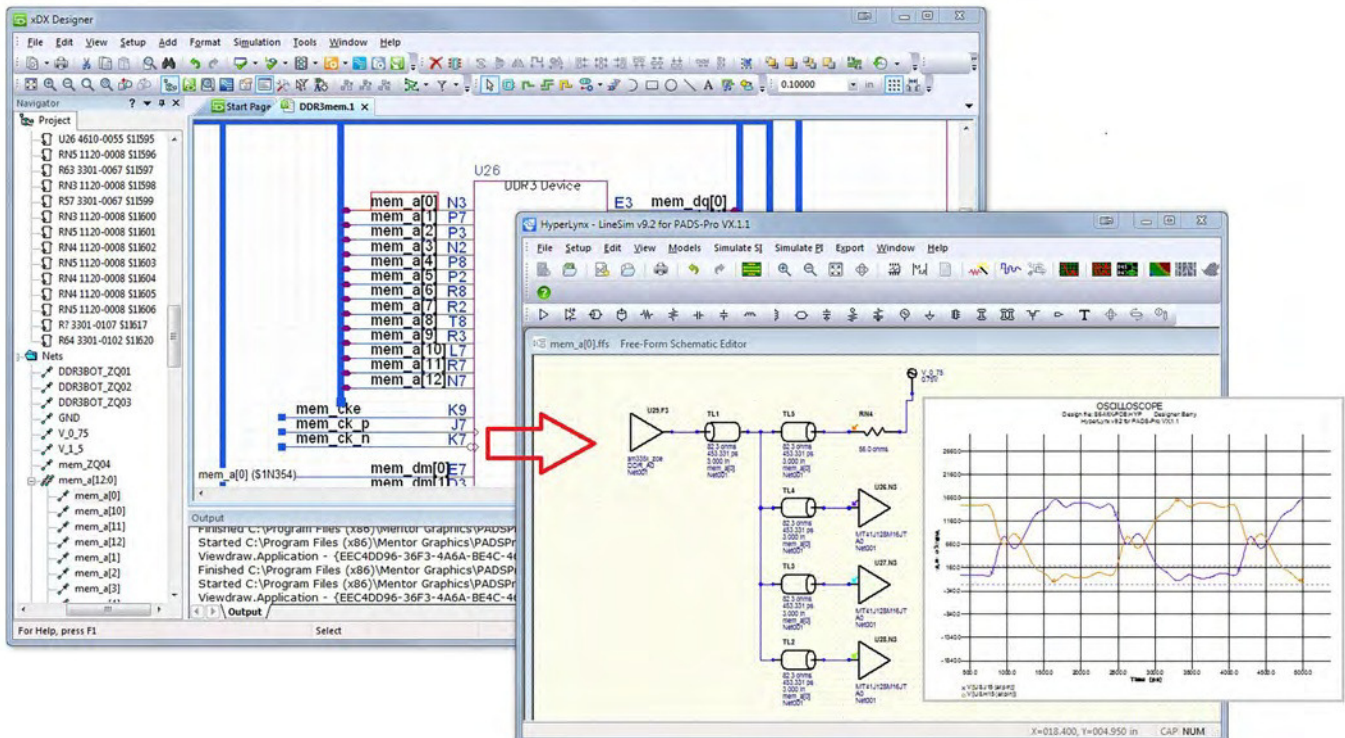


Figure 1: Develop high-speed design constraints based on pre-layout simulation (xDX Designer to HyperLynx).

To begin with, every designer needs a set of well-established design rules to base the constraints on. IPC has provided the electronics industry with guidelines for designing and manufacturing PCBs compiled over the years with the support of both committee and industry members.

The IPC-2220-FAM: Design Standard for Printed Boards series is the bible for PCB designers. The series is built around IPC-2221B—the base document that covers all generic requirements for PCB regardless of materials. From here, the designer chooses the appropriate sectional standard for a specific technology.

The IPC-2220-FAM series includes:

- IPC-2221B: Generic Standard on Printed Board Design
- IPC-2222A: Sectional Design Standard for Rigid Organic Printed Boards
- IPC-2223C: Sectional Design Standard for Flexible Printed Boards
- IPC-2224: Sectional Standard for Design of PWBs for PC Cards
- IPC-2225: Sectional Design Standard for Organic Multichip Modules (MCM-L) and MCM-L Assemblies
- IPC-2226A: Sectional Design Standard for High-density Interconnect (HDI) Printed Boards

This series provides coverage on material and final finish selection, current-carrying capacity and minimum electrical clearances, test-specimen design, guidelines for V-groove scoring, dimensioning requirements, and conductor thickness requirements.

Also, several documents apply to HSD and land-pattern design:

- IPC-2141A: Design Guide for High-speed Controlled Impedance Circuit Boards
- IPC-2251: Design Guide for Electronic Packaging Utilizing High Speed Techniques
- IPC-7351B: Generic Requirements for Surface Mount Design and Land Pattern Standard

These standards (and their predecessors)

have been part of a well-used section of my technical library since 1987. They provide excellent reading and reference material for all PCB designers. These documents are available for purchase from www.ipc.org.

Design rules must keep up with the latest devices and fabrication processes without losing sight of design for manufacturability (DFM). DFM is the practice of designing board products that can be produced in a cost-effective manner using existing manufacturing processes and equipment. If you follow the above IPC guidelines, you will be designing for both manufacturability and mass production. However, at times, one must stretch the rules a little to meet the specific requirements of a design. This is fine, providing you can justify the reasons and tolerate the consequence of your decision.

Entry-level EDA tools tend to rely on the skills of the PCB designer to detect possible issues as they arise during the design process. However, these days, a more constraint-driven, correct-by-construction approach is required for complex designs. Once the rules are established, they will be followed by downstream tools and validated to conform by the various design rule checkers (DRCs). A spreadsheet format is more efficient if you are dealing with a high volume of constraints, sorting, filtering, and duplicating constraints.

Constraint management:

- Enables better synchronization between schematic and layout
- Streamlines access to relevant PCB data
- Eliminates errors due to data integrity issues
- Promotes greater reuse of PCB data

Figure 2 illustrates typical constraints planning and definition for a high-speed DDR2 and DDR3 design. Constraints should be defined at the schematic level and flow through to the layout process. The advantage of this approach is that the engineer can convey their intent to the PCB designer without misinterpretation. Alternatively, the independent engineer (who does everything) can manage the constraints

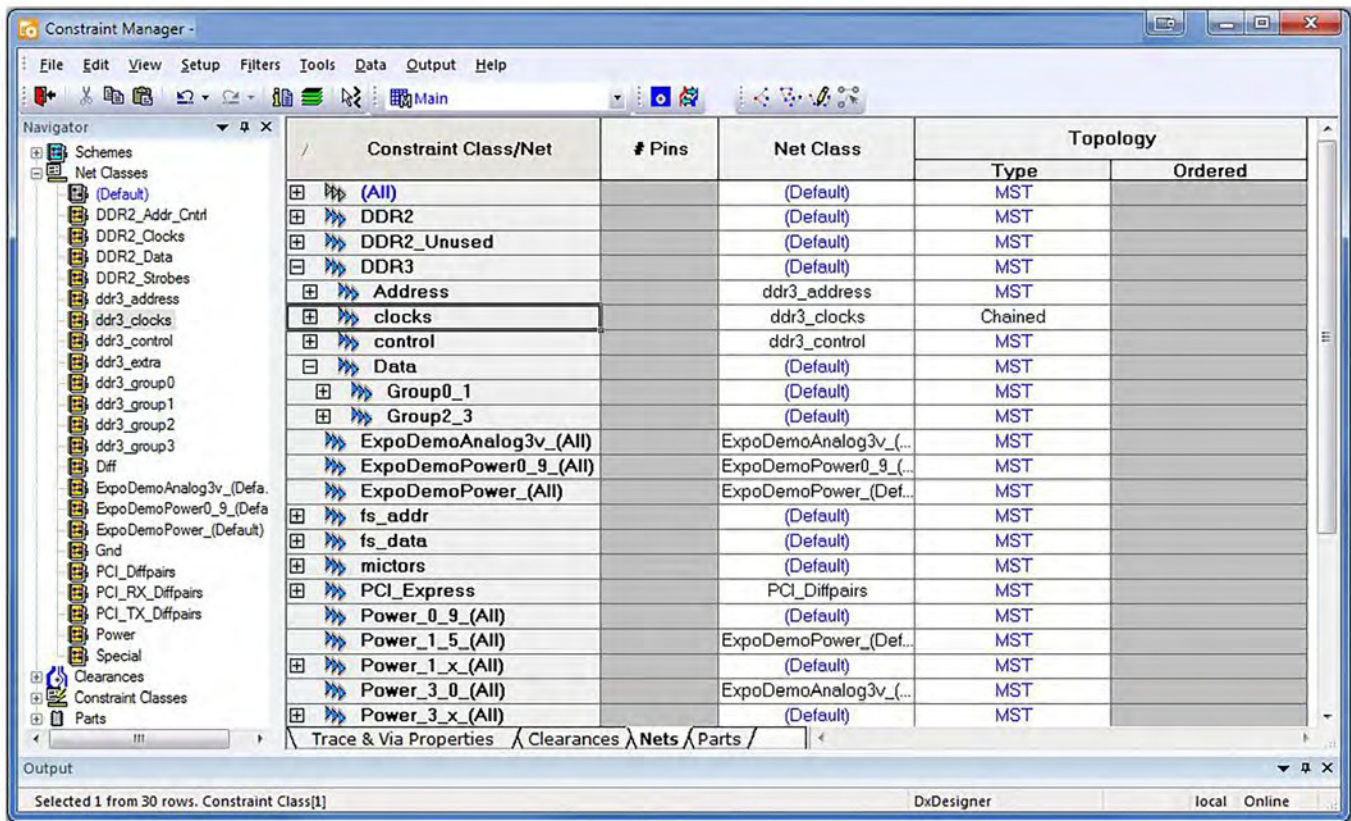


Figure 2: Constraints planning at the schematic level (PADS Professional).

throughout the design process using the same consistent management tool. Also, the reuse of constraints from a previous proven design not only ensures consistent rules but also minimizes the possibility of errors.

Net classes are used to organize and speed up the definition of routing constraints for nets with similar properties. For each net class, the layers allowed for routing, the corresponding trace width range for these layers, and the via types allowed can be defined. For differential pairs, a layer-dependent differential pair gap can be defined based on the calculated impedance to ensure uniform impedance across all layers.

The proper grouping and definition of net classes and constraint classes in the early stages of the design process simplifies constraint definition and management significantly. Grouped constraints can increase layout efficiency, reducing design time, and, ultimately, lower PCB design costs.

With DDRx design, it is also a requirement to assign layer sets to data lanes/strobes and ad-

dress, command, and control (ACC) and their associated clocks to ensure matched propagation delay. Signals within a group should be routed on the same layer with each path having the same via count. Even if the trace widths are adjusted on each layer, so as the impedance is identical, the propagation speed of microstrip (outer layer) is always faster than stripline (inner layer), typically by 13–17% (Figure 3). The speed of propagation of digital signals is independent of trace geometry and impedance and is solely determined by the dielectric constant of the material the electromagnetic energy propagates in.

The higher the signal frequency with which the designer must contend, the more complicated will be the PCB design. Complex PCB designs require deep knowledge and experience and simulation tools. However, it is not always necessary to route traces as short as possible, differential signals as close as possible, or to avoid crosstalk as much as possible. Rather, it depends on the signal's significance. Basically, the designer must know which are the sensi-

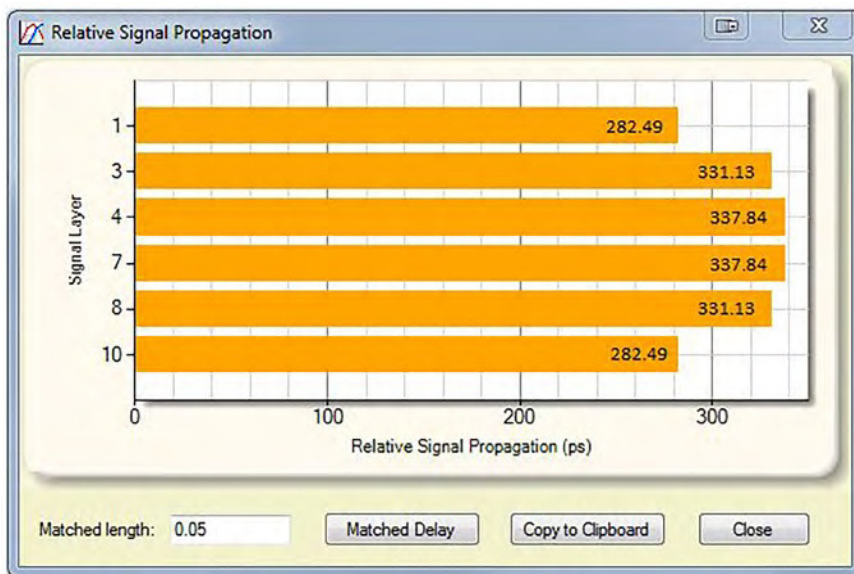


Figure 3: Relative signal propagation of microstrip and stripline (iCD Design Integrity).

tive parts in the circuit or where problems due to reflections and crosstalk can occur. With this knowledge, good placement of the devices can be made. Because placement is such an important step in high-speed design, the designer will do well always to keep it and the return current in mind.

With higher frequencies and faster transition times, the digital system timing budget is also of the utmost importance. The timing budget is the account of timing requirements necessary for a system to function properly. For synchronous systems to work, timing requirements must fit within one clock cycle. A timing budget calculation involves many factors, including setup and hold time and maximum operating frequency requirements. By calculating a timing budget, the limitations of conventional clocking methods can be seen. This data can then be translated into routing design constraints.

The first step in establishing the timing budget is to define the initial system timings. To do this, one must obtain estimates of the minimum and maximum output skew from the silicon vendors. This information is generally available in the IC datasheets. Then, define the setup and hold times for the read and write cycles. The timing budget for each component is then calculated given a certain margin. What-

ever is left over (if anything) can then be allocated to the board-level interconnect design. This is the only factor that PCB designers can influence. If there is no margin left for the interconnect, then the silicon numbers need to be retargeted, or an easier solution might be to decrease the clock speed. This is why a shoddy design may work at a low frequency but not at full speed. Timing is everything in high-speed design.

In conclusion, PCB designers need to understand the underlying high-speed design issues of the design based on simulation and then translate these

into corresponding design constraints. Constraints can always be altered on the fly if a particular constraint is too tight, providing the designer can justify the easing of the specification and that the product is still manufacturable.

Key Points:

- The key methodology is to understand the underlying high-speed design issues and then translate these into corresponding design constraints
- High-speed design constraints are based on pre-layout simulation
- Constraint reuse is limited by net and group naming conventions; if you are consistent, then porting is much easier
- IPC has provided the electronics industry with guidelines for designing and manufacturing PCBs
- Entry-level EDA tools tend to rely on the skills of the PCB designer to detect possible issues as they arise during the design process
- A constraint-driven, correct-by-construction approach is required for complex designs
- Constraints should be defined at the schematic level and flow through to the layout process

- The proper grouping and definition of net classes and constraint classes in the early stages of the design process simplifies constraint definition and management significantly
- The propagation speed of microstrip (outer layer) is always faster than stripline (inner layer), typically by 13–17%
- The speed of propagation of digital signals is independent of trace geometry and impedance and is solely determined by the dielectric constant of the material
- The designer must know which are the sensitive parts in the circuit or where problems due to reflections and crosstalk can occur
- The timing budget is the account of timing requirements necessary for a system to function properly
- The timing budget shows the limitations of conventional clocking methods and can then be translated into routing design constraints **DESIGN007**

Further Reading

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Barry Olney is managing director of In-Circuit Design Pty Ltd (iCD), Australia, a PCB design service bureau that specializes in board-level simulation. The company developed the iCD Design Integrity software incorporating the

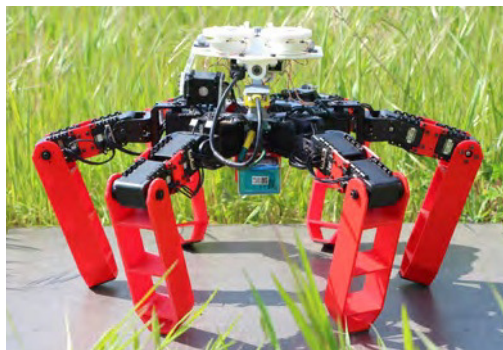
iCD Stackup, PDN, and CPW Planner. The software can be downloaded from www.icd.com.au. To read past columns or contact Olney, [click here](#).

The First Walking Robot that Moves Without GPS

Researchers at CNRS and Aix-Marseille University (AMU), in the Institut des Sciences du Mouvement—Étienne Jules Marey (ISM), have designed the first walking robot that can move without GPS: AntBot.

Inspired by desert ants—which are considered extraordinary solitary navigators—AntBot can explore its environment randomly and go home automatically without GPS or mapping.

Ants use polarized light and ultraviolet radiation to locate themselves in space. Cataglyphis desert ants, in particular, can cover several hundreds of meters in direct sunlight in the desert to find food, then return in



a straight line to the nest without getting lost. Distance and heading are the two fundamental pieces of information that, once combined, allow them to return smoothly to the nest.

AntBot is equipped with an optical compass used to determine its heading by means of polarized light, and an optical movement sensor directed to the sun to measure the distance covered. Armed with this information, AntBot has been shown to be able to explore its environment and to return on its own to its base with a precision of up to one cm after having covered a total distance of 14 m.

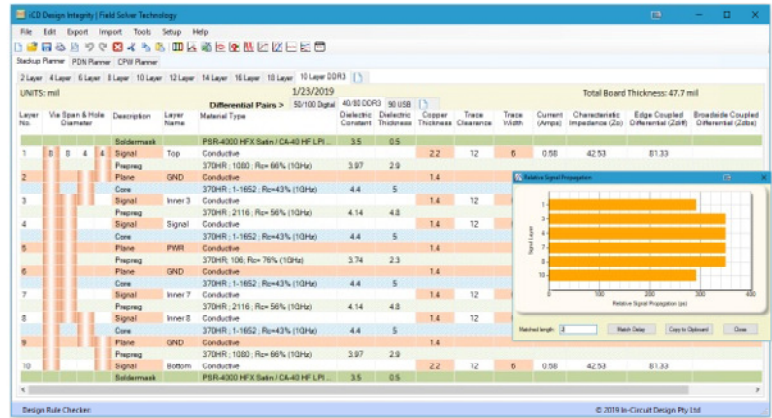
(Source: French National Centre for Scientific Research)

iCD Design Integrity

iCD Stackup Planner

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 Relative signal propagation delay
 iCD Termination Planner
 iCD Materials planner
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 Dielectric Materials Library >33,000
 Interfaces to Allegro, Altium, Excel,
 HyperLynx, OrCAD, PADS, Xpedition,
 Zmetrix TDR, Zuken and IPC-2581B

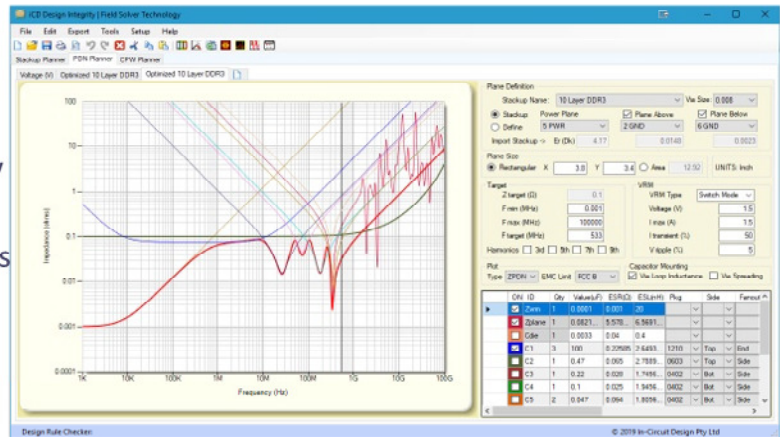
Offers Engineers and PCB Designers unprecedented simulation speed, ease of use and accuracy at an affordable price



iCD PDN Planner

AC impedance analysis with resonance
 Integration of stackup plane data
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 decaps and mounting loop inductance
 PDN EMI Plot with FCC and CISPR Limits
 Extensive Capacitor Library >5,650
 Capacitor S-Parameter model import

Analyze multiple power supplies to maintain low impedance over entire frequency range dramatically improving product performance



iCD CPW Planner

Reduces radiation loss
 Fast Coplanar Waveguide analysis
 Model single and dual (differential)
 CPWs plus a dual Coplanar Strip (CPS)
 Characteristic impedance and
 edge-coupled differential impedance
 Optional Dielectric Materials Library

Model microstrip Coplanar Waveguides to reduce radiation loss, of high-speed serial links, significantly improving product performance

