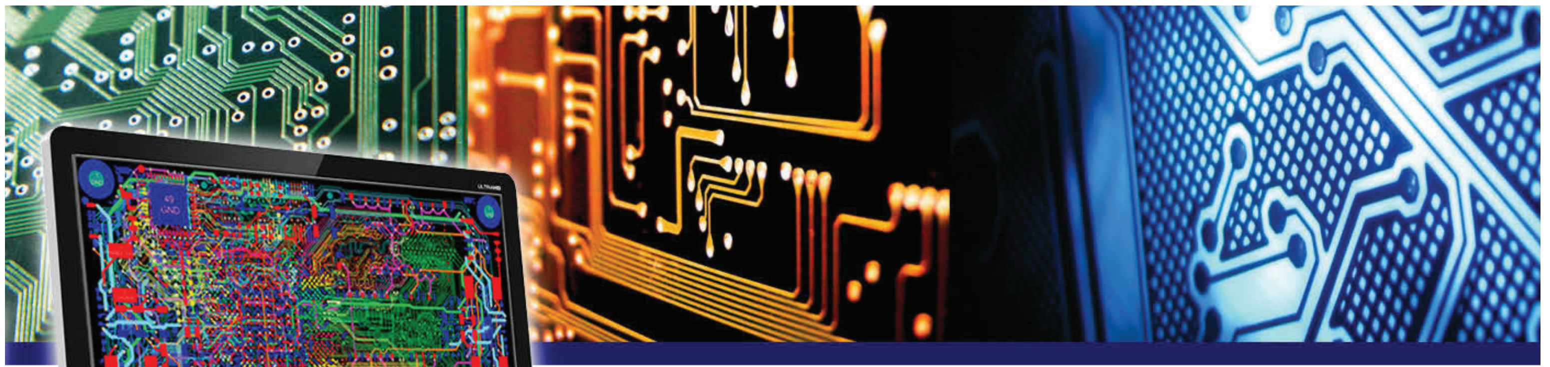

BOARD LEVEL SIMULATION SPECIALISTS

ICD Stackup Planner - offers engineers/PCB designers unprecedented simulation speed, ease of use and accuracy at an affordable price

- 2D (BEM) field solver precision
- Characteristic impedance, edge-coupled & broadside-coupled differential impedance
- Unique field solver computation of multiple differential technologies per stackup
- Heads-up impedance plots of signal and dielectric layers
- User defined dielectric materials library - over 16,250 materials up to 100GHz

ICD PDN Planner - analyze multiple power supplies to maintain low impedance over entire frequency range dramatically improving product performance

- Fast AC impedance analysis with plane resonance
- Definition of plane size/shape, dielectric constant & plane separation for each on-board power supply
- Extraction of plane data from the integrated Stackup Planner
- Definition of voltage regulator, bypass/decoupling capacitors, mounting loop inductance
- Frequency range up to 100GHz
- Extensive Capacitor Library – over 5,250 capacitors derived from SPICE models

iCD

In-Circuit Design Pty Ltd

LEARN MORE

www.icd.com.au

PCB Design Techniques for DDR2 & DDR3

by Barry Olney
In-Circuit Design Pty Ltd, Australia

SUMMARY

This second and last part in a series examining PCB Design Techniques will look at the comparison of DDR2 to DDR3; DDR3 design guidelines; pre-layout analysis; critical placement; an example of design rules; and finally, the post-layout analysis.

One major difference between DDR2 and DDR3 SDRAM is the use of levelling. To improve signal integrity and support higher frequency operations, the JEDEC committee defined a fly-by termination scheme used with the clocks, command and address bus signals. Fly-by topology reduces simultaneous switching noise (SSN) by deliberately causing flight-time skew between the data and strobes at every chip/DRAM, requiring controllers to compensate for this skew by adjusting the timing per byte lane (Table 1).

During a write, DQS groups are launched at separate times to coincide with a clock

DDR2/DDR3 Comparison	**DDR2**	**DDR3**
Max Clock Frequency	533/1066	800/1600
ODT	Static	Dynamic
VDD	1.8V	1.5V (may also be 1.35V)
VTT	0.9V	0.75V
Vref	0.9V	0.75V
Input thresholds	0.9V	0.75V
Match Addr/CMD/CTRL to CLK tightly	yes	yes
Match DQ/DMO/DSQ tightly	yes	yes
Match DQS to clock loosely	yes	not required

Table 1.

“ IN GENERAL, TRY TO KEEP THE SDRAM AS CLOSE AS POSSIBLE TO THE CONTROLLER, BUT BEAR IN MIND THAT SOMETIMES IT WILL NOT BE NOT POSSIBLE BECAUSE OF OTHER PHYSICAL CONSTRAINTS. ”

arriving at components on the DIMM/PCB, and must meet the timing parameter between the memory clock and DQS defined as tDQSS of ± 0.25 tCK.

The design process can be simplified using the new levelling feature of DDR3 and controller IC’s. The fly-by daisy chain topology increases the complexity of the data path and controller design to achieve levelling, but also greatly improves performance and eases board layout for DDR3.

DDR3 Design Guidelines— Critical Constraints:

- Clock nets, DQ (data) and DQS (strobes) are routed differentially. 4.5” max length +/- 25MIL
- Net length from driver to first DIMM or chip: between 2” to 3” max depending on load
- Net length between DIMM’s or chips: 0.5”
- Net length from last DIMM or Chip to the VTT Termination: 0.2” to 0.55”
- All DSQ/DQ (data and data strobe) should be minimized to reduce the skew within groups (or lanes) and across groups. 50 MIL within groups and 800 MIL across groups.
- Skew between address nets should be 200MIL. Address and command nets are daisy chained with a VTT pull-up for termination.

Other constraints to consider:

- DDR3 data nets have dynamic On-Die Termination (ODT) built into the controller and SDRAM. The configurations are 40Ω, 60Ω and 140Ω so VTT pull-up is not necessary.
- Zo for DDR3 is 50Ω. Zdiff is 100Ω.

Pre-layout Analysis

I can’t emphasize enough the importance of pre-layout analysis. Without which, you are just relying on luck—which is not a design parameter. The pre-layout simulation is used to predict and eliminate signal integrity issues early, proactively constraining routing and optimizing clock, critical signal topologies and terminations prior to board layout.

As previously mentioned, the value and placement of the series resistors and VTT pull-ups for data, address and command signals depends on the distances between the loads, number of loads and the stackup of the board and are best determined by simulation. The series terminator may not be required if a single SDRAM is used and the trace length is short—but how do you know if you don’t simulate the proposed layout?

In general, try to keep the SDRAM as close as possible to the controller, but bear in mind that sometimes it will not be not possible because of other physical constraints. Also, if there are two or more SDRAM chips, this becomes more difficult and requires extended signal lengths terminators. Now the question becomes, where should they be placed and what values should be used?

The series terminator would normally be placed close to the driver. Surprisingly, however, in the above case, the signal integrity

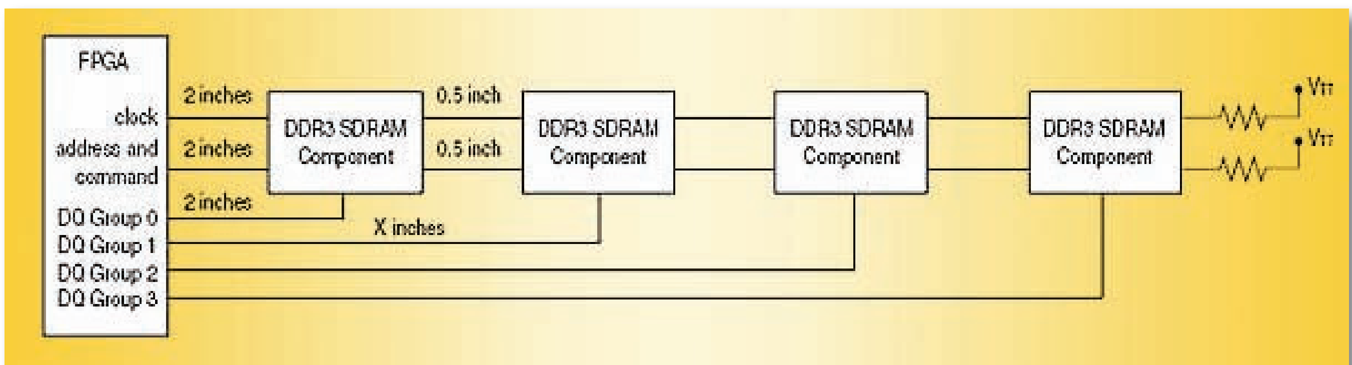

Figure 1: 2.375<x<2.652” DDR3 topology using levelling.

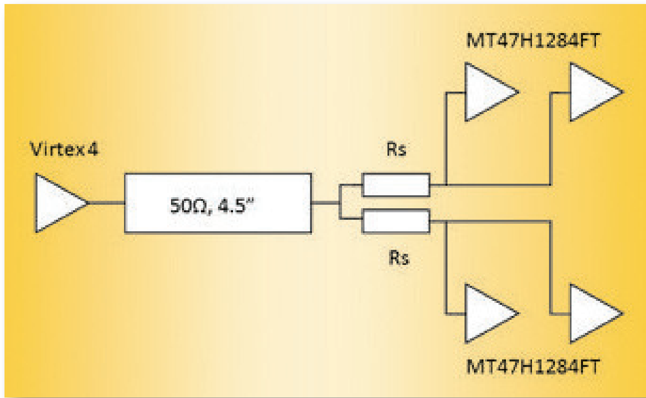

Figure 2: In this design, signal integrity will be better if the series terminator is placed 4.5" away from the driver.

was much better with a long distance (4.5 inches) away from the driver, and then the signal split through two series resistors and into each bank of DDR2 SDRAM. This is unusual, but demonstrates the importance of simulation in order to achieve the best possible outcome. By the way, this design ran at full rate with no rework required.

Placement

If you have completed the pre-layout analysis, then placement is a matter of following the constraints determined for length and placement rules. Series terminators are normally placed in RESNET 1206 (4 resistor packages) or 0402 on the bottom of the board, as the top is typically taken up by large active devices.

Decaps should be placed directly beneath the devices where possible, using 20 MIL traces connected to the supply pins to reduce inductance. It is sometimes possible to use the vias coming down from fine pitch BGA supply pins as one pin for the 0402 Decap and routing the other to ground.

Matched Length and Differential Pair Routing

Setting up the design rules is a little tedious in any PCB tool, but, once done on the first design, you can export them into the next design to save time. Below (Table 2) is an example of DDR2 High-Speed Design Rules for Altium Designer.

When possible, I normally reduce the tolerance within Data Lanes 0-3 to 25 MIL in order to get a tighter match, although the JEDEC Spec is 50 MIL. These special high-speed design rules should be given top priority in the design rule hierarchy.

Final Post-Layout Analysis

The final post-layout analysis includes a batch mode simulation of all the nets. This flags signal integrity, crosstalk and EMI hot spots. Basically, look carefully through this report to see any issues that may have to be dealt with.

The batch mode simulation reports:

- Signal Integrity issues including over/under shoot.
- Nets that are too long and need termination.
- Crosstalk from multiple aggressor nets.
- Possible EMI sources.

Go through these items one at a time and look at whether there needs to be action taken. For instance, a long 'Reset' signal or a signal going to a static pull-up may be reported as being too long, but we can obviously ignore these particular warnings. Another possible case that needs to be addressed: a critical signal that is routed over the Manhattan length and needs termination.

Crosstalk is quite common in high speed designs because of the cramped real estate; signals have to be packed tightly into a small area. Crosstalk can be minimized by increasing trace spacing and by reducing the signal layer to reference plane separation. Try to keep prepreg thickness to 3 MIL to tightly couple the signals to the plane. Also, it may be necessary to add additional planes to the stackup to isolate the offending aggressor signals. Routing adjacent signal layers orthogonally also helps reduce noise coupling.

Crosstalk problems can cause intermittent operation due to timing glitches and interference, dramatically reducing your product's reliability. So, it is best to address these issues at the source.

If a good job has been done routing the high-speed signals, on the internal layers and away from the edges of the board, then EMI should be minimal. However, if there is an EMI

Rule Name	Rule Type	Scope	Atttribute
Length	Length	(InNetClass('Lane0') AND InNetClass('Lane1') AND InNetClass('Lane2') AND InNetClass('Lane3'))	Min Length = 500mil Max Length = 1000mil
Parallel Segment	Parallel Segment	All - All	Gap = 4mil Limit = 500mil Layer = Same Layer
USB Data and Control	Matched Net Lengths	InNetClass('USB_length')	Tolerance = 100mil
Diff Pair USB Matched Lengths	Matched Net Lengths	InDifferentialPair ('USB')	Tolerance = 25mil
Diff Pair Matched Lengths	Matched Net Lengths	(InDifferentialPairClass ('All Differential Pairs'))	Tolerance = 25mil
DDR CLK Matched Lengths	Matched Net Lengths	InDifferentialPair ('DDR_MCK')	Tolerance = 25mil
DDR2 CTL	Matched Net Lengths	InNetClass('DDR2_CTL')	Tolerance = 200mil
DDR2 Addr	Matched Net Lengths	InNetClass('DDR2_Addr')	Tolerance = 200mil
Lane3	Matched Net Lengths	InNetClass('Lane3')	Tolerance = 50mil
Lane2	Matched Net Lengths	InNetClass('Lane2')	Tolerance = 50mil
Lane1	Matched Net Lengths	InNetClass('Lane1')	Tolerance = 50mil
Lane0	Matched Net Lengths	InNetClass('Lane0')	Tolerance = 50mil
All Lanes	Matched Net Lengths	(InNetClass('Lane0') AND InNetClass('Lane1') AND InNetClass('Lane2') AND InNetClass('Lane3'))	Tolerance = 500mil

Table 2.

issue then different routing strategies can be tried to eliminate the problem. EMC can be measured, during the design process, to FCC, CISPR, VCCI Class A & B standard—this alone saves multiple iterations of a design.

All critical high-speed signals should be individually checked. Signal flight times need to be within spec, and eye diagrams need to have eyes wide open.

By simulating during the design process, you can be assured that your PCB layout will be of the highest quality and will pass the relevant EMC tests—saving you time, money and frustration for a fraction of the cost of board iterations and multiple compliancy testing. Plus, the simulation can be done before the design is finalized (before Gerber output or even earlier in the design process) to further reduce production time and costs. **PCB**

References:

1. Advanced Design for SMT – Barry Olney, In-Circuit Design Pty Ltd.

2. JEDEC Specifications JESD 79F, JESD79-2E & JESD79-3D.

3. Altera Board Layout Guidelines, EMI_Plan_Board.

Barry Olney is Managing Director of In-Circuit Design Pty Ltd (ICD), Australia, a PCB Design Service Bureau and Board Level Simulation Specialist. Among many other awards through the years, ICD was awarded "Top 2005 Asian Distributor Marketing" and "Top 2005 Worldwide Distributor Marketing" by Mentor Graphics, Board System Division.