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Design Techniques for DDR2 & DDR3 Part 1

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SUMMARY

In the first part of this two-part article on PCB design techniques for DDR, DDR2 and DDR3, we will look at the pre-layout setup of typical DDRx designs considering the multilayer PCB stackup, technology rules and how they should be selected, and the power distribution network and associated decoupling, and introduce the design rules for DDR and DDR2 layout.

Multilayer PCB Stackup

Before starting the PCB design it is important to plan the PCB stackup. To achieve the best results, the following points need to be taken into account:

- a) Technology Rules—trace width, clearance—characteristic and differential impedance.
- b) The Power Distribution Network (PDN)— which power planes are required?
- c) Bypass and Decoupling.
- d) Return Paths of Matched Length Signals— one point that is generally missed.

a) Technology Rules

The technology rules are based on the minimum pitch of the BGA components employed and are basically the largest trace, clearance and via allowable while minimizing PCB fabrication costs. Technology of 4/4 MIL (trace/clearance) and vias of 20/8 MIL (pad/hole) are generally required.

Once these rules have been established, calculate the stackup required for the desired characteristic impedance (Z_o) and the differential impedance (Z_{diff}). These are $Z_o = 50\Omega$ and $Z_{diff} = 100\Omega$ for DDRx (DDR has $Z_o = 60\Omega$). Keep in mind that lower impedance will increase the dI/dt and dramatically increase the current drawn (not good for the PDN) and higher impedance will emit more EMI and also make the design more susceptible to outside interference. So, a good range of Z_o is 50Ω to 60Ω .

Also, keep in mind that USB differential signals may be used on the board. These require a Z_{diff} of 90Ω . So, the trace width and clearance need to be adjusted for these signals.

How do you calculate the Z_o and Z_{diff} of the entire stackup using the established design rules?

Well, this one I have made easy for you. In-Circuit Design Pty Ltd has developed the ICD Stackup Planner which is ideal for this. You can download an evaluation copy from www.icd.com.au.

“ THE CORE DC SUPPLIES MUST FIRST BE IDENTIFIED AND FOR EACH OF THESE SUPPLIES CALCULATE THE MAXIMUM DC CURRENT (SINK) REQUIRED. ”

b) The Power Distribution Network (PDN)

As you may be aware, there are many different power supply requirements for the DDRx controllers, FPGA or CPUs. The core DC supplies must first be identified and for each of these supplies calculate the maximum DC current (sink) required. For instance, 5 amps may be required, for a 20 degree rise in temperature of the substrate, so the design rules need to be set to reflect this requirement. The ICD Stackup Planner can also be used to obtain these calculations.

Then, finding a way to deliver the supplies to the BGAs is the next drama. It will usually be necessary to split the power planes to accommodate all of these supplies. This can be done providing the power plane isn't used for the return path of the DDRx signals. It is preferable to locate these core fills directly under the controller.

c) Bypass and Decoupling

A bypass capacitor acts by dampening the AC or noise on the supply. As simultaneous switching signals draw high current, the DC supply tends to have noise imposed onto it. And to make it worse, the latest IC's are very sensitive to noise due to the lowering of supply voltages and the presence of a large number of potential noise generators.

Decoupling capacitors supply instantaneous current (at different frequencies) to the drivers until the power supply can respond. In other words, it takes a finite time for current to flow from the power supply circuit (whether on board or remote) due to the inductance of the trace and/or wires to the drivers.

It is best to follow the chip manufacturer's recommendations on the numbers, values and position of these capacitors, although it is quite daunting to be asked to place three or four decaps on each supply pin. This will be discussed in more detail in the placement section.

d) Return Paths and Matched Length Signals

One point that always amazes me: Designers generally take great care to ensure that matched length signals are routed exactly to length from the driver to the DDRx device pin, but take no care of the return path of the

signal. Current flow is a 'round trip.' If it takes one signal longer for the return current to get back to the driver (around a gap in the plane for instance) then there will be skew between the critical timing signals.

So, when you plan your stackup, be aware of which plane(s) (either power or ground) will be the return path for your critical signals and make sure there is an unobstructed return path.

DDRx Specifications and Design Rules

The DDRx Specs can be downloaded from www.jedec.org. These are at first quite daunting with many pages of requirements for timing budgets, matched length, differential pair and de-rating of setup and hold times.

DDRx JEDEC Specifications

DDR	JESD 79F
DDR2	JESD79-2E
DDR3	JESD79-3D

These devices are SDRAM that use Double Data Rate (DDR) architecture to achieve high-speed operation by transferring two data words per clock cycle at the I/O pins.

DDR Design Guidelines—Critical Constraints:

- Net length from driver to first DIMM or chip—between 2" to 6" depending on load. There may need to be a series terminator depending on the load and net length.
- Net length between DIMM's or chips—0.4" to 1.2"
- Net length from last DIMM or Chip to the VTT Termination—0.5" to 2"
- All DSQ/DQ (data and data strobe) should be minimized to reduce the skew within groups (or lanes) and across groups. 15 MIL within groups and 15 MIL across groups.

Other constraints to consider:

- Clock nets are routed differentially.
- Data nets may need a series termination between the driver and first DIMM or chip.

Note: DIMMs also have a series resistor after the connector.

- Address and command nets may need a series termination and are daisy chained with a VTT pull-up for termination.
- Zo for DDR is 60Ω.

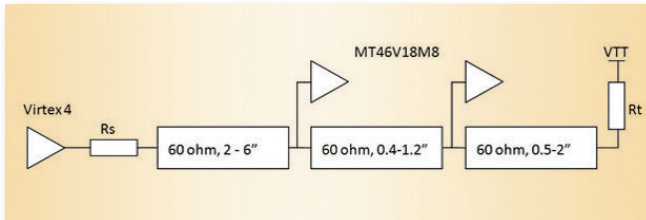


Figure 1: Address, Data and Command nets may need series and VTT termination.

The value and placement of the series resistors and VTT pull-ups for data, address and command nets depends on the distances between the loads, number of loads and the stackup of the board, and are best determined by simulation. The series terminator may not be required if a single SDRAM is used and the trace length is short.

Also, the routing layers should be selected such that each net has a common reference plane(s), for the return path of the signal, and routed internally (where possible) to reduce EMI. Stitching vias or capacitors can be used to connect reference planes. With any high-speed board, crosstalk should be analyzed to reduce interference.

DDR2 Design Guidelines—Critical Constraints:

- Net length from driver to first DIMM or chip—between 1.9" to 4.5" depending on load
- Net length between DIMMs or chips—0.425"
- Net length from last DIMM or Chip to the VTT Termination—0.2" to 0.55"
- All DSQ/DQ (data and data strobe) should be minimized to reduce the skew within groups (or lanes) and across groups. 50 MIL within groups and 500 MIL across groups.
- Skew between address nets should be 200 MIL. Address and command nets are

daisy chained with a VTT pull-up for termination.

Also other constraints to consider:

- Clock nets and DQS (data strobes) are routed differentially.
- Data nets may need a series termination between the driver and first DIMM or chip.
Note: DIMM's also have a series resistor after the connector.
- DDR2 data nets have On Die Termination (ODT) built into the controller and SDRAM. The configurations are 50Ω, 75Ω and 150Ω, so VTT pull-up is not necessary.
- Zo for DDR2 is 50Ω. Zdiff is 100Ω.

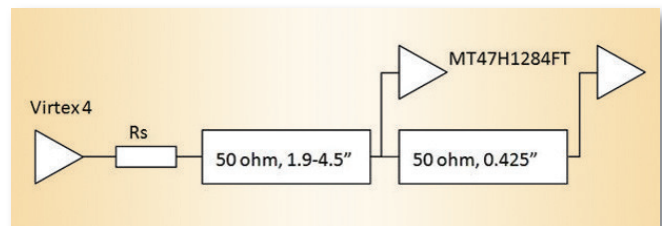


Figure 2: DQ (data) has no VTT termination.

The second and last part of the article will look at the comparison of DDR2 to DDR3; DDR3 design guidelines; pre-layout analysis; critical placement; an example of design rules; and finally, the post-layout analysis. **PCB**

References:

- Advanced Design for SMT—Barry Olney, In-Circuit Design Pty Ltd.
- JEDEC Specifications JESD 79F, JESD79-2E & JESD79-3D.
- Altera Board Layout Guidelines, EMI_Plan_Board.



Barry Olney is Managing Director of In-Circuit Design Pty Ltd (ICD), Australia, a PCB Design Service Bureau and Board Level Simulation Specialist. Among many other awards through the years, ICD was awarded "Top 2005 Asian Distributor Marketing" and "Top 2005 Worldwide Distributor Marketing" by Mentor Graphics, Board System Division.