

The Curse of the Golden Board

Beyond Design

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At DC and low frequencies, the inductance of transmission line paths can be ignored. However, as the frequency and rise time increase, we soon realize that the multilayer PCB is not an ideal environment to transfer high-speed data. Here, parasitic capacitance and inductance plague the most basic of designs. Inductance, in particular, impacts on virtually all signal and power integrity issues.

To optimize the physical layout for acceptable performance, inductance must be minimized:

1. The mutual inductance between signal paths intensifies switching noise
2. The inductance of the power distribution network (PDN) bypass and decoupling capacitors dramatically affects product performance and reliability
3. The effective loop inductance of the return current paths impacts on electromagnetic (EM) emissions

By understanding how the physical PCB layout influences the degree of inductance, the PCB designer can triumph over their arch-enemy.

Electric fields and magnetic fields play an equal role in moving energy in a multilayer PCB. EM fields also move energy in free space but not at DC. The presence of voltage implies that there is an electric field, and the changing of that electric field creates a magnetic field. What may not be appreciated is that moving a voltage between two components requires moving energy (not a signal), which requires the existence of both electric and magnetic fields. When energy is not moving, the magnetic field is zero.

1. Mutual Inductance Between Signal Paths

When current flows in a conductor, there is a magnetic field. When a second conductor, carrying current, is brought into close proximity, there is a force between the two. If both cur-

rents flow in the same direction, then they are additive (think two parallel trace segments). When the currents flow in the opposite direction (think a trace over a return plane), the currents cancel. This implies that two individual traces should be kept well apart to reduce crosstalk whilst a signal trace should be tightly coupled to its return path (plane) to increase coupling and reduce inductance.

Parasitic inductance is often an afterthought in high-speed design. A substrate consisting of conducting and dielectric materials will have some parasitic inductance, possibly leading to problems like crosstalk, induced currents, noise coupling, and other effects that degrade signal quality.

Unfortunately, parasitic capacitance and inductance in a PCB are unavoidable. A PCB is composed of a number of parallel conducting elements that are separated by an insulator, basically forming a capacitor. Likewise, conductors on a PCB will inevitably form complete loops, creating an equivalent inductor. While making dielectric layers in the stackup thinner will decrease the loop area and the parasitic inductance, it will also increase parasitic capacitance. Therefore, one needs to choose the sweet spot where inductance is minimized, and capacitance is maximized.

In high-speed digital applications where multiple data lines can run at tens of Gbps, parasitic

capacitance and inductance can produce impedance mismatch along the signal path. Any mismatch caused by parasitics will produce reflections along the transmission line, ultimately increasing timing jitter and bit error rates.

Figure 1 shows the near (NEXT) and far-end (FEXT) crosstalk for the victim traces adjacent to the aggressor trace (1.5V at 1 GHz). In this case, the traces are 4 mils wide with 4-mil spacing and have a 40-ohm impedance. As the victim trace gets farther away from the aggressor, the crosstalk decreases. The self-inductance line rings are those field line rings around a trace that arise from its own current only, whilst the mutual inductance line rings are the magnetic field line rings completely surrounding a trace that arise from another trace's current; these cause the crosstalk. Crosstalk creates ringing, which creates electromagnetic radiation.

2. Inductance of the Power Distribution Network

Also, as the frequency and rise times increase, the AC impedance of the PDN increases due to the inductance of the bypass and decoupling capacitors attached to the planes. Every capacitor has an equivalent series inductance (ESL), which causes its impedance to increase at high frequencies. Bulk bypass capacitors provide low impedance up to ~ 10 MHz. High-frequency decoupling is provided by ceramic capacitors up to several hundred MHz, but above that, only the planar capacitance can reduce the PDN impedance. The power-to-ground plane capacitance of the PCB provides an ideal capacitor in that it has no series lead inductance and little equivalent series resistance (ESR), which helps reduce noise at extremely high frequencies, providing tight coupling (< 5 mils) between planes creates valuable capacitance at high frequencies.

Capacitors reach their minimum impedance at their resonant frequency (Figure 2), which is determined by the capacitance, ESR, and ESL. To meet the PDN target impedance at a particular frequency, a capacitor is chosen so that when mounted on the PCB, it will resonate at the desired frequency and have an impedance

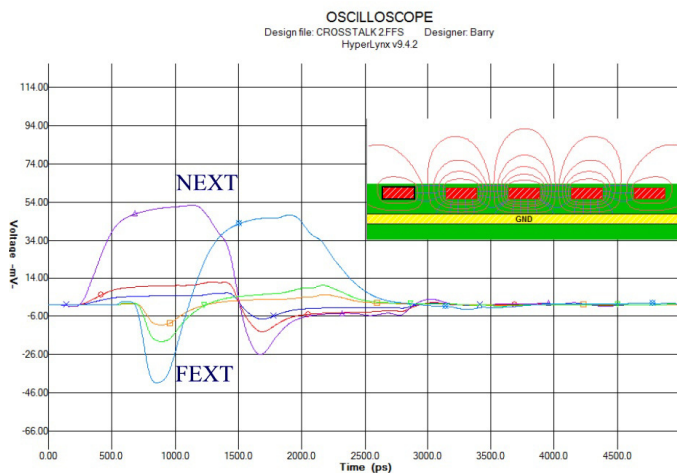


Figure 1: Near and far-end crosstalk for microstrip (simulated in HyperLynx).

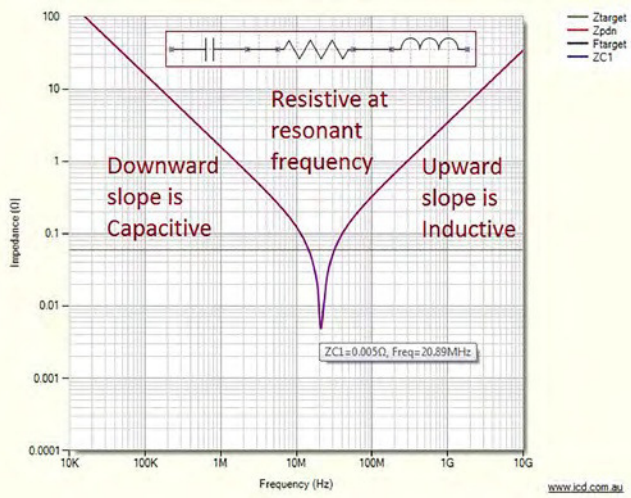


Figure 2: A capacitor has series capacitance, resistance, and inductance (iCD PDN Planner).

that is equal to its ESR. Then, a sufficient number of those capacitors are placed in parallel so that the accumulated ESR's approach the desired target impedance.

In addition, the mounting inductance of a capacitor is comprised of three components: capacitor footprint, capacitor height above or below the plane, and power plane spreading inductance. These three elements describe the loop that current must flow; the bigger the loop, the more the inductance. The footprint (land pattern) for a capacitor dominates the ESL. It consists of via placement with respect to the

pad, the length and width of traces connected to the pad, and the way the vias are connected to the power and ground planes. The location of the power/ground planes in the PCB stack-up controls the length of the vias; this is why it is always best to place the decoupling capacitors on the same side of the board as the BGA for high layer-count stackups. Inductance directly depends on the magnetic field, so reducing the energy associated with the loop area reduces overall inductance.

Figure 3 illustrates 0402 capacitors with different fanout patterns. End vias are the worst case where the loop area (inductance) is the largest. This loop area can be reduced by placing the vias closer to the land side and even more so by placing double vias either side of the pad basically halving the inductance. The final case is that of via-in-pad, which reduces the loop area dramatically, but caution should be used as not all assembly shops support this. Placing double vias has approximately the same inductance as using the via-in-pad. Also, vias should be directly connected to the plane rather than by thermal reliefs, which adds to the inductance.

3. Loop Inductance of the Return Paths

PCB designers, generally, take great care to ensure that critical signals are routed exactly to

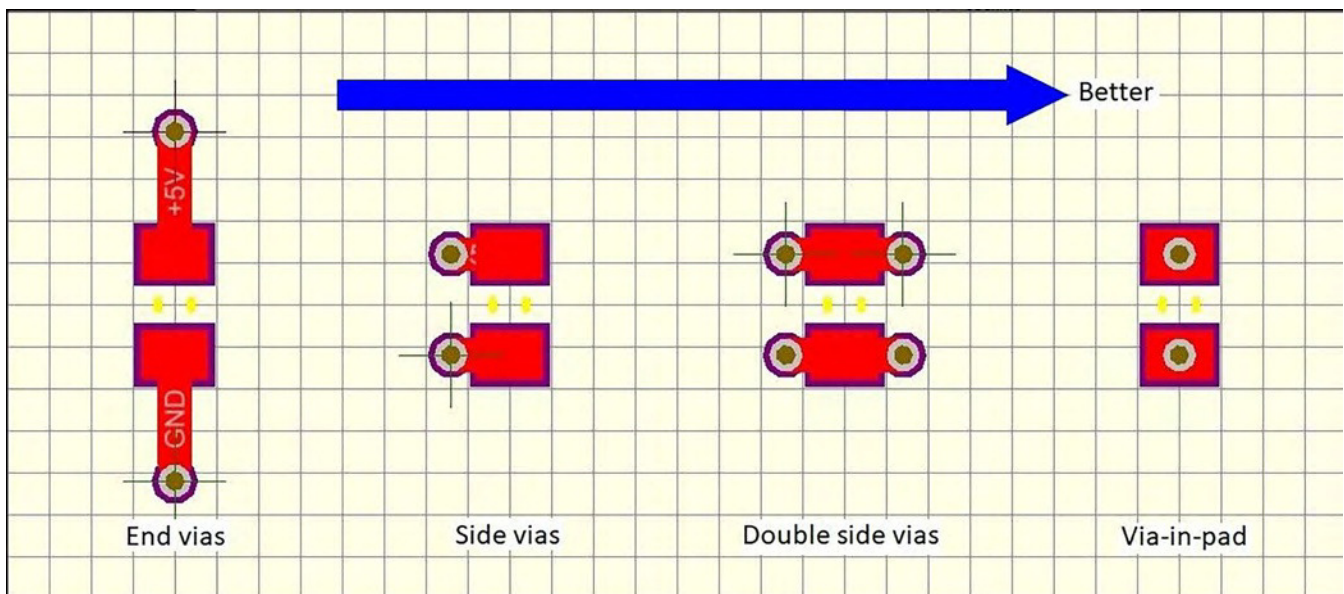


Figure 3: Capacitor mounting and via fanout.

length from the driver to the receiving device pins but take little care of the return current path of the signal. Current flow is a round trip, and the important issue is delay, not length. If it takes one signal longer for the return current to get back to the driver—such as around a gap in the plane—then there will be skew between the critical timing signals. Return path discontinuities (RPDs) can also create large loop areas that increase series inductance, degrade signal integrity, and increase crosstalk and electromagnetic radiation.

Small discontinuities, such as vias and non-uniform return paths on a bus, are becoming an important factor for the signal integrity and timing of high-speed systems. RPDs produce impedance discontinuities due to the local return inductance and capacitive changes. Impedance discontinuities create reflected noise, contribute to differential channel to channel noise, and may promote mode conversion. In the case of differential pairs, the transformation from differential-mode to common-mode typically takes place on bends, and non-symmetrical routing near via and pin obstructions, but can also be caused by small changes in impedance due to RPDs.

Common mode radiation is the result of parasitics in the circuit, which emanate from the unwanted voltage drops in the conductors. As the signal is driven down the transmission line, capacitive coupling between the trace and plane conductors completes the loop and displacement current flows through the capacitance which returns to the source. The common-mode current that flows through the ground impedance produces a voltage drop in the digital logic ground system and generates magnetic radiation.

To control common mode radiation, it is important to minimize the common mode ground voltage at the source. Also, good grounding minimizes noise sources by presenting common mode currents with a low impedance path to ground potential. If the return path of a common mode current is far from the signal path, then the common mode current will radiate. However, if you engineer the return path to be in close proximity to the source current,

then the loop area will be small; therefore, the common mode current will not radiate.

In conclusion, parasitic effects can be minimized by separating traces as much as possible, coupling signal traces close to the reference planes, reducing the loop area of return current, using good stackup design practices, and lowering the AC impedance of the PDN by minimizing the decoupling capacitor mounting inductance.

Key Points

- Inductance, in particular, impacts virtually all signal and power integrity issues
- Moving a voltage between two components requires moving energy (not a signal), which requires the existence of both electric and magnetic fields
- Two individual traces should be kept well apart to reduce crosstalk whilst a signal trace should be tightly coupled to its return path (plane) to increase coupling and reduce inductance
- Parasitic capacitance and inductance in a PCB are unavoidable
- Parasitic capacitance and inductance can produce impedance mismatch along the signal path
- As the frequency and rise times increase, the AC impedance of the PDN increases due to the inductance of the bypass and decoupling capacitors attached to the planes
- The power to ground plane capacitance, of the PCB, provides an ideal capacitor in that it has no series lead inductance and little equivalent series resistance, which helps reduce noise at extremely high frequencies
- Capacitors reach their minimum impedance at their resonant frequency
- A capacitor is chosen so that when mounted on the PCB, it will resonate at the desired frequency
- The footprint (land pattern) for a capacitor dominates the ESL
- The location of the power/ground planes in the PCB stackup controls the length of the vias; this is why it is always best to

place the decoupling capacitors on the same side of the board as the BGA for high layer-count stackups

- Capacitor mounting loop area can be reduced by placing the vias closer to the lands
- Vias should be directly connected to the plane rather than by thermal reliefs, which adds to the inductance
- Current flow is a round trip, and the important issue is delay, not length
- Return path discontinuities can also create large loop areas that increase series inductance
- RPDs produce impedance discontinuities due to the local return inductance and capacitive changes
- If the return path of a common mode current is far from the signal path, then the common mode current will radiate

Further Reading

- Olney, B. “Beyond Design: Crosstalk Margins,” *Design007 Magazine*, July 2018.
- Olney, B. “Beyond Design: Power Distribution Network Planning,” *The PCB Magazine*, May 2012.
- Olney, B. “Beyond Design: PDN Planning and Capacitor Selection, Part 1,” *The PCB Design Magazine*, December 2013.

- Olney, B. “Beyond Design: PDN Planning and Capacitor Selection, Part 2,” *The PCB Design Magazine*, January 2014.
- Olney, B. “Beyond Design: Return Path Discontinuities,” *The PCB Design Magazine*, April 2017.
- Olney, B. “Beyond Design: Common Symptoms of Common-Mode Radiation,” *Design007 Magazine*, May 2018.
- Morrison, R. *Fast Circuit Boards: Energy Management*, John Wiley & Sons, 2018.
- Cadence PCB Solutions. “How Parasitic Capacitance and Inductance Affect Your Signals,” Cadence Design Systems Inc., May 2, 2019.
- Bogatin, E. *Signal and Power Integrity: Simplified*, Prentice Hall, 2008.
- Johnson, H. W., & Graham, M. *High-Speed Digital Design: A Handbook of Black Magic*, Prentice Hall, 1993. **DESIGN007**



Barry Olney is managing director of In-Circuit Design Pty Ltd. (iCD), Australia, a PCB design service bureau that specializes in board-level simulation. The company developed the iCD Design Integrity software incorporating the iCD Stackup, PDN, and CPW Planner. The software can be downloaded www.icd.com.au. To read past columns or contact Olney, [click here](#).

Cooling for Quantum Electronics

The startup kiutra GmbH is the first company in the world to have succeeded in developing a permanent magnetic cooling system to reach temperatures close to absolute zero. Such temperatures are, for example, required for the operation of quantum computers. The system was set up by a team of researchers from the Physics Department at the Technical University of Munich (TUM).

TUM researchers Alexander Regnat, Jan Spallek, Tomek Schulz, and Professor Christian Pfleiderer are seeking to meet that demand. All four are currently working on their prototype at the TUM Physics Department. According to Alexander Regnat, there is already the prospect of taking on more staff and setting up separate headquarters.

The team of scientist came up with the idea during their

work at the TUM. Again and again, they were faced with the limits of conventional methods for reaching such low temperatures. Therefore, the group developed its own technology to ensure permanent cooling and founded kiutra GmbH in the summer of 2018.

Concepts for permanent magnetic cooling have been around for many years. “However, technical implementation is extremely challenging, and this has previously prevented the development of a product for widespread use,” explains Schulz.

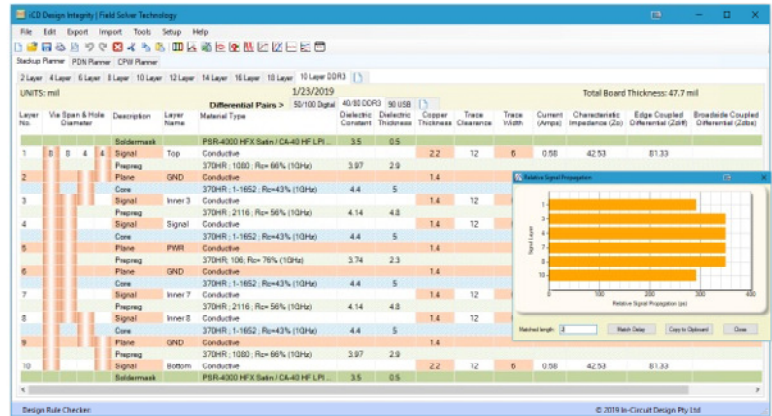
“We are the world’s first commercial supplier of a cooling system that can magnetically achieve temperatures close to absolute zero (near -273°C) on a permanent basis,” says Regnat. (Source: Science and Technology Research News)

iCD Design Integrity

iCD Stackup Planner

Precision 2D (BEM) field solver
 Controlled impedance analysis
 Relative signal propagation delay
 iCD Termination Planner
 iCD Materials planner
 Multiple differential technologies
 Heads-up impedance plots
 Dielectric Materials Library >33,000
 Interfaces to Allegro, Altium, Excel,
 HyperLynx, OrCAD, PADS, Xpedition,
 Zmetrix TDR, Zuken and IPC-2581B

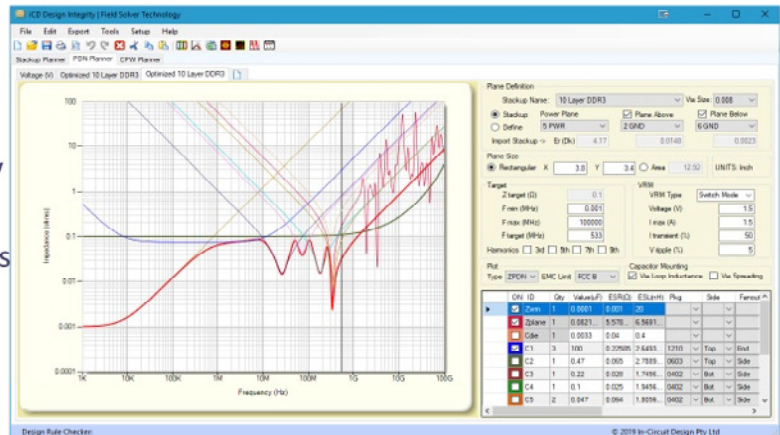
Offers Engineers and PCB Designers unprecedented simulation speed, ease of use and accuracy at an affordable price



iCD PDN Planner

AC impedance analysis with resonance
 Integration of stackup plane data
 Definition of voltage regulator, bypass/
 decaps and mounting loop inductance
 PDN EMI Plot with FCC and CISPR Limits
 Extensive Capacitor Library >5,650
 Capacitor S-Parameter model import

Analyze multiple power supplies to maintain low impedance over entire frequency range dramatically improving product performance



iCD CPW Planner

Reduces radiation loss
 Fast Coplanar Waveguide analysis
 Model single and dual (differential)
 CPWs plus a dual Coplanar Strip (CPS)
 Characteristic impedance and
 edge-coupled differential impedance
 Optional Dielectric Materials Library

Model microstrip Coplanar Waveguides to reduce radiation loss, of high-speed serial links, significantly improving product performance

