

# BOARD LEVEL SIMULATION SPECIALISTS

ICD Stackup Planner - offers engineers/PCB designers unprecedented simulation speed, ease of use and accuracy at an affordable price

- 2D (BEM) field solver precision
- Characteristic impedance, edge-coupled & broadside-coupled differential impedance
- Unique field solver computation of multiple differential technologies per stackup
- Heads-up impedance plots of signal and dielectric layers
- User defined dielectric materials library - over 16,250 materials up to 100GHz

ICD PDN Planner - analyze multiple power supplies to maintain low impedance over entire frequency range dramatically improving product performance

- Fast AC impedance analysis with plane resonance
- Definition of plane size/shape, dielectric constant & plane separation for each on-board power supply
- Extraction of plane data from the integrated Stackup Planner
- Definition of voltage regulator, bypass/decoupling capacitors, mounting loop inductance
- Frequency range up to 100GHz
- Extensive Capacitor Library – over 5,250 capacitors derived from SPICE models

# Controlling Emissions and Improving EMC

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This application note discusses Electromagnetic Compliancy (EMC) fundamentals and common approaches and methodologies to suppress unintentional noise

## Basic Definitions

Electromagnetic Interference (EMI)

- Radiation can produce electromagnetic interference.
- Any electromagnetic disturbance that interrupts, obstructs, or otherwise degrades or limits the effective performance of electronics and electrical equipment. It can be the result of spurious emissions and responses.

Electromagnetic Compliancy (EMC)

- The ability of equipment to be used in its intended environment without causing or receiving degradation due to unintentional EMI.
- The ability to comply with standards related to the levels of EMI associated with a particular product.

## EMC Standards

In Australia, we comply with the CISPR standard that is also the European standard. The United States complies to the FCC and in Japan the VCCI standard.

The two classes or levels of radiation and conducted emissions limits for unintentional radiators are specified for example in FCC Part 15 Subpart B. Class A - digital devices, the higher less strict limits, and Class B - digital devices, the lower more strict limits. Manufacturers are encouraged to meet the Class B digital device limits.

These standards define the maximum amount of noise or interference that the equipment can generate and also the immunity or susceptibility of the equipment to outside interference of transient voltages and RF fields of different magnitudes and frequency.



In Australia and New Zealand we have the following certification trademarks:

1. C-Tick is a certification trademark for the AS/NZS CISPR 22:2002
2. A-Tick mark illustrates compliance with both the EMC and telecommunications requirements in Australia, but only with EMC requirements in New Zealand

EMI sources can be external or internal to a system or board. An example of an external EMI source is RF power from a mobile (cell) phone (which can radiate both back into the phone or into other systems).

The most common types of internal EMI sources are clocks, high speed data lines, and large di/dt variations due to high-speed digital logic.

The three elements of an EMC issue:

1. Source – obviously the noise emanates from a source on the PCB. Emissions can be reduced after EMC testing by applying ferrites to cables etc but it is best to totally eliminate, control or attenuate the emissions at the source.
2. Coupling Path – A trace and its return path generate differential mode radiation or a trace with no return path generates common mode radiation acting like an antenna converting current into electromagnetic radiation. The noise can be radiated, conducted or induced via the coupling path to the victim.
3. Receiver – Radiation is coupled into a receiver or ‘victim’. The victim could be a trace with no return path or a cable etc.

As previously mentioned, it is best to totally eliminate, control or attenuate the emissions at the source. In an ideal design, the respective loads into which each of the signal sources are connected would consume all of the signal energy switched during the driving of the transmission line. Therefore, no energy would be available for radiation as noise.

This can be achieved by terminating each signal source into a load equal to its source impedance; the condition required for maximum transfer of power. The connecting interfaces must exhibit zero loss, and have transmission line impedance equal to their respective source and load impedances. When these conditions are met, the load would absorb 100% of the power from all signal sources, and no signal energy (noise) would be radiated.

So the best place to start then is to control the impedance of the PCB substrate. This can be done by calculating the characteristic and differential impedances of the stackup.

A typical eight layer board stackup is shown below (Fig. 1). The Characteristic and Differential Impedances of the substrate are calculated using the ICD Stackup Planner (available for download @ [www.icd.com.au](http://www.icd.com.au)).

ICD STACKUP PLANNER – www.icd.com.au												6/9/2011	Total Board Thickness: 1517
UNITS: um													
Layer	Material	Dielectric		Copper		Trace		Current	Impedance	Edge Coupled	Broadside Coupled	Description	
Number	Name	Type	Constant	Thickness	Thickness	Clearance	Width	(Amps)	Characteristic(Zo)	Differential(Zdiff)	Differential(Zdbs)		
1	Top	Dielectric	3.3	12.7								Soldermask	
		Conductive			17	127	127	0.22	59.76	99.69		Signal	
		FR408 2116 (180 Tg)	3.7	99								Prepreg	
2	GND	Conductive			17							Plane	
		FR408 (180 Tg)	3.7	152								Core	
3	Inner 3	Conductive			17	127	127	0.22	49.99	88.16		Signal	
		FR408 2116 (180 Tg)	3.7	99								Prepreg	
		FR408 2113 (180 Tg)	3.7	74								Prepreg	
4	VDD	Conductive			17							Plane	
		FR408 (180 Tg)	3.7	533								Core	
5	GND	Conductive			17							Plane	
		FR408 2116 (180 Tg)	3.7	99								Prepreg	
		FR408 2113 (180 Tg)	3.7	74								Prepreg	
6	Inner 6	Conductive			17	127	127	0.22	49.99	88.16		Signal	
		FR408 (180 Tg)	3.7	152								Core	
7	VCC	Conductive			17							Plane	
		FR408 2116 (180 Tg)	3.7	99								Prepreg	
8	Bottom	Conductive			17	127	127	0.22	59.76	99.69		Signal	
		Dielectric	3.3	12.7								Soldermask	

Fig. 1

This stackup is ideal for high speed digital designs and can be used as a 'safe bet' if you are risk averse or a first time high speed designer.

The substrate is produced from Isola FR408 dielectric material. FR408 is a high-performance FR-4 epoxy laminate & prepreg system designed for advanced circuitry applications. Its low Dielectric Constant (Dk) and low Dissipation Factor (DF) make it an ideal candidate for broadband circuit designs requiring faster signal speeds or improved signal integrity. FR408 also brings the board reliability with its high glass transition temperature (Tg).

FR408 has the following advantages over standard FR-4 material:

- Improved Dielectric Properties. DK less than 3.8 (50MHz - 1GHz) - Supports increased signal speeds.
- DF less than 0.010 (50MHz - 1GHz) - Provides better signal integrity.
- Glass Transition Temperature of 180 degrees Celsius – Supports higher reflow temperatures and improves solder joint reliability.

Once the stackup has been planned to control the impedance of the transmission lines, the drivers need to be matched to the loads. This is typically done using a series (backmatching) resistor but pre-layout simulation should be used to determine exactly if and what value of resistor is required.

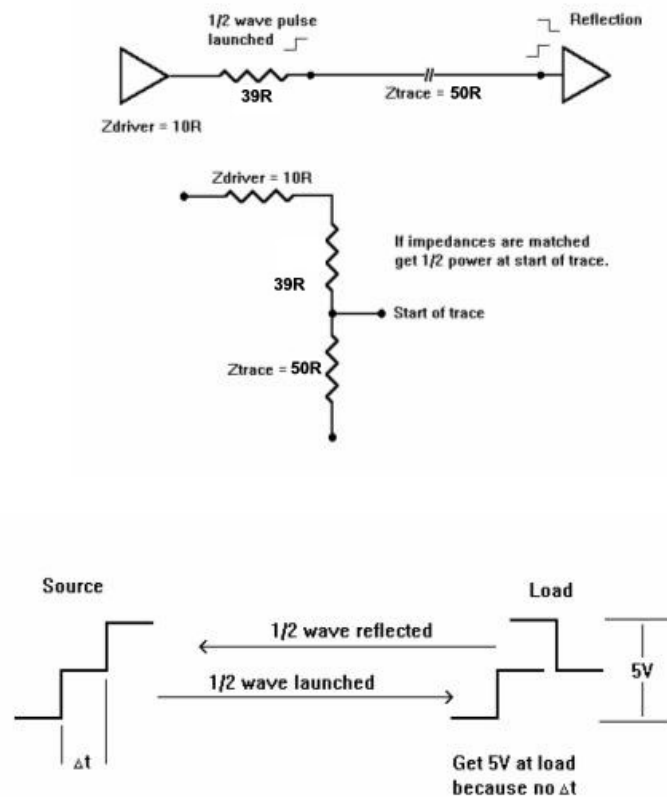


Fig. 2

Impedance backmatching slows down the rise and fall times and reduces the ringing (over/under shoot) of clock drivers (typically a 22 to 39 ohm resistor is used). The source impedance plus the backmatching resistor must equal the transmission line impedance in order to launch a  $\frac{1}{2}$  wave pulse into the transmission line. This pulse is then instantaneously reflected back from the high input impedance load creating a nearly perfect square wave at the load.

When do you need to backmatch a driver?

**Rule of thumb:** All drivers whose length (in inches) is equal to or greater than the rise and fall time (in nS) must have provision for termination.

So, if you have a 1nS rise time on your clock – one inch (25.4 mm) is the maximum distance that it can be routed without backmatching.

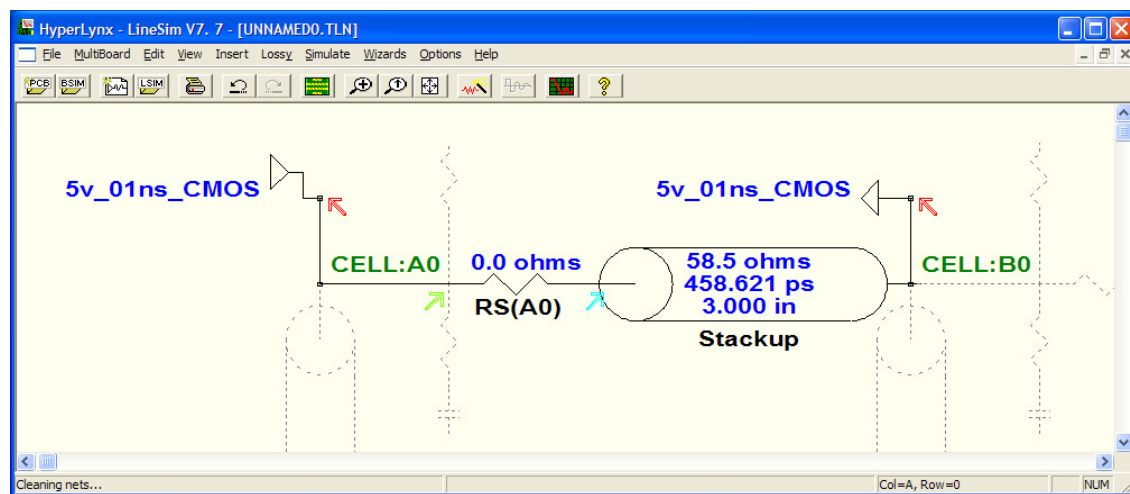


Fig. 3

Fig. 3 shows the transmission line model of a 5V, 1nS source and load with a 3 inch, 458pS, 58.5 ohm transmission line.

The red signal of Fig. 4 shows the ringing of the transmission line without termination. The green signal shows the transmission line with a 33 ohm series backmatching resistor RS(A0) added close to the source. Notice how most of the noise is eliminated when the source and load are more closely matched to the impedance of the line.

If this noise is not constrained then it will be coupled into nearby victim traces (crosstalk) and radiated to create EMI. Apart from the issues of EMI, signal integrity and crosstalk this noise can cause intermittent operation of the product due to timing glitches and interference dramatically reducing the products reliability.

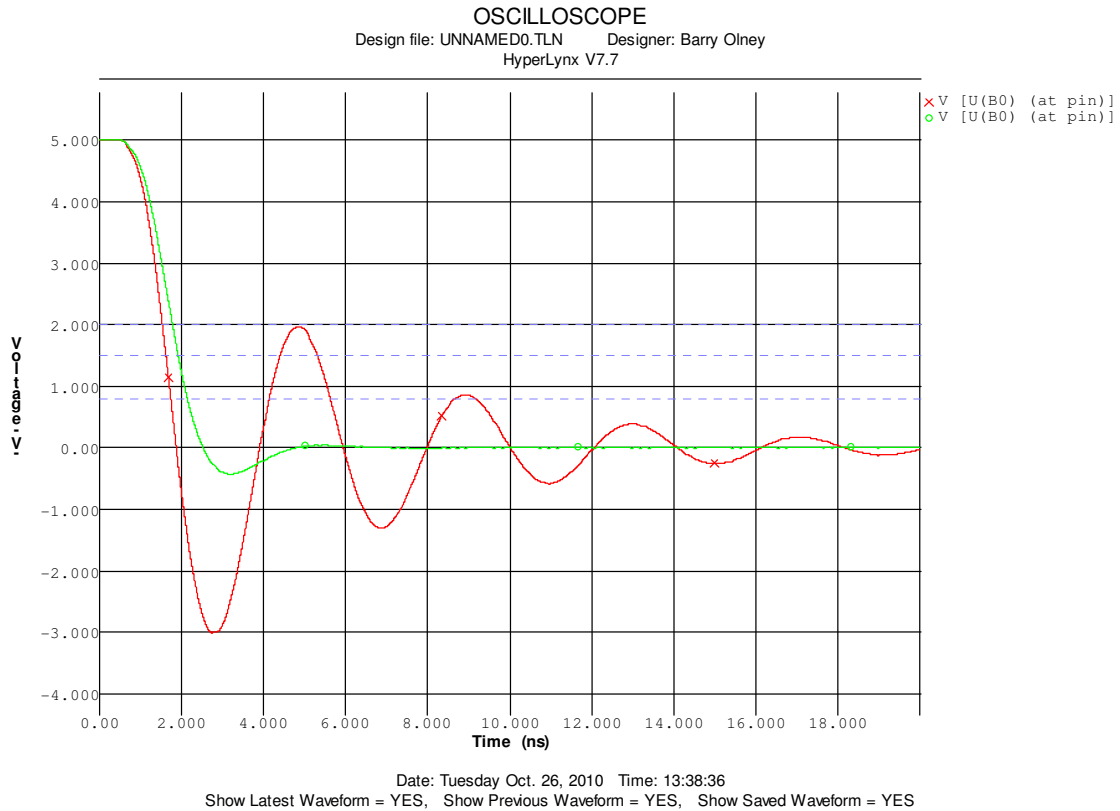


Fig. 4

This crosstalk (noise) can also be reduced by increasing the space between the victim and aggressor nets (by at least three times the trace width) and by reducing the signal layer to plane layer spacing of the substrate.

In conclusion, controlling the impedance of the substrate and terminating the transmission line to match the impedance of the respective source and load significantly reduces radiated noise virtually eliminating the noise at the source.

**References:**

- Advanced Design for SMT – Barry Olney, In-Circuit Design Pty Ltd
- Design for EMC – Barry Olney, PCD Magazine January 1996
- The ICD Stackup Planner can be downloaded from [www.icd.com.au](http://www.icd.com.au)

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