Beyond Design – Controlled Impedance Design

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Controlled Impedance – it's all about transmission lines. For perfect transfer of energy, the impedance of the driver must match the transmission line. A good transmission line is one that has constant impedance along the entire length of the line, so that there are no mismatches resulting in reflections. But unfortunately, drivers do not have the exact impedance to match the line (typically 10 – 35 ohms) so terminations are used to balance the impedance, match the line and minimize reflections.

Reflections occur whenever the impedance of the transmission line changes along its length. This can be caused by unmatched drivers/loads, layer transitions, different dielectric materials, stubs, vias, connectors and IC packages. By understanding the causes of these reflections and eliminating the source of the mismatch, a design can be engineered with reliable performance.

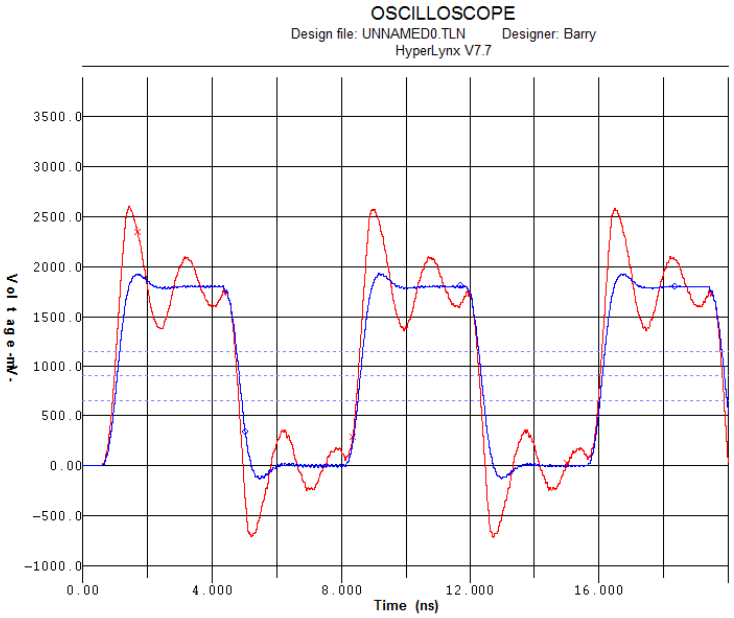

Figure 1 – Unterminated (red) vs terminated (blue) transmission lines

Impedance matching slows down the rise and fall times, reduces the ringing (over/under shoot) of clock drivers and enhances the signal quality of a high-speed design. The ringing is dramatically reduced by adding a series terminator as in Figure 1. From this, we can see that the impedance has to be matched – but to what value?

For a microstrip transmission line with 3mil dielectric thickness to ground, a 9mil trace width is required to match a DDR3 34 ohm driver. Have you ever tried routing matched length DDR3 with 9mil traces – that ain't gunna work. If the driver's impedance is even lower, say 22 ohms, then you would need to route 15mil traces.

Figure 2 illustrates the plot of impedance vs microstrip trace width (left) and impedance vs dielectric thickness (right). These plots are simulated by multiple passes of the field solver (in the background) to create heads-up graphs of how to adjust the particular variables to achieve the desired impedance. One can see, that as the impedance goes down, the trace width increases to a point where it will be unrouteable. Also, if we select too low an impedance, the di/dt will increase drawing excessive current from the supply, no doubt creating further power integrity issues.

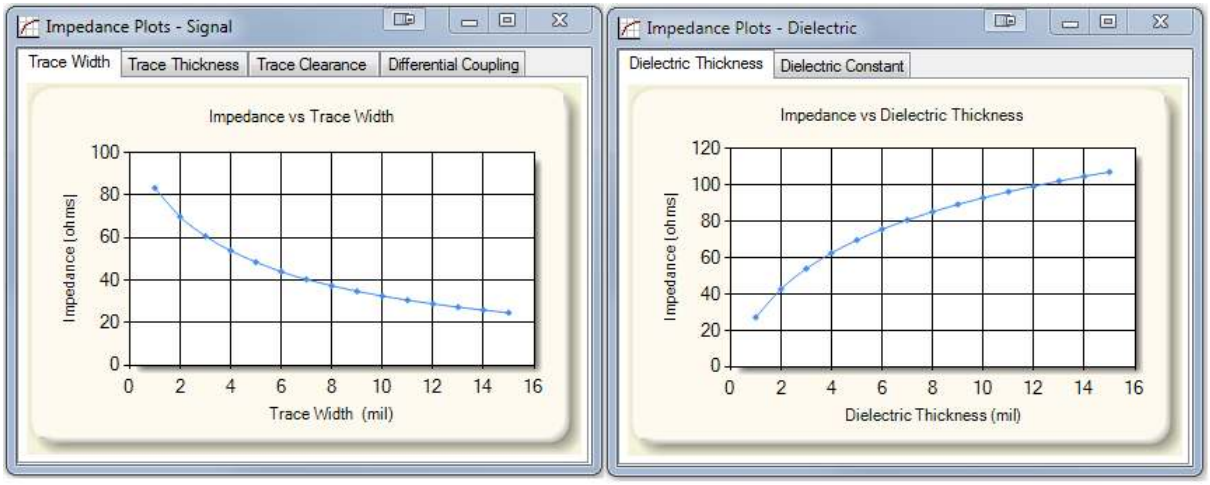

Figure 2 – the ICD Stackup Planner's impedance plots

So, it is a trade-off between trace width, trace (copper) thickness, dielectric thickness and dielectric constant. Then if you also need to include differential impedance, then the trace clearance also comes into play. Plus, one needs to also consider what the preferred fab shop has in stock. So determining the correct variable, for your application, is not as simple as clicking an impedance 'goal seeking' button. But rather, one should weigh up all the pros and cons of changing each variable and make an informed decision. That is exactly what the impedance plots allow you to determine.

Also, as the dielectric constant and loss of all materials varies with frequency, the impedance needs to be simulated at the frequency of the highest bandwidth taking into account the 5th harmonic. Traditional, dielectric constant and loss has been measured at 100MHz but these days a 1GHz (or higher) frequency is more appropriate to be used to determine the impedance.

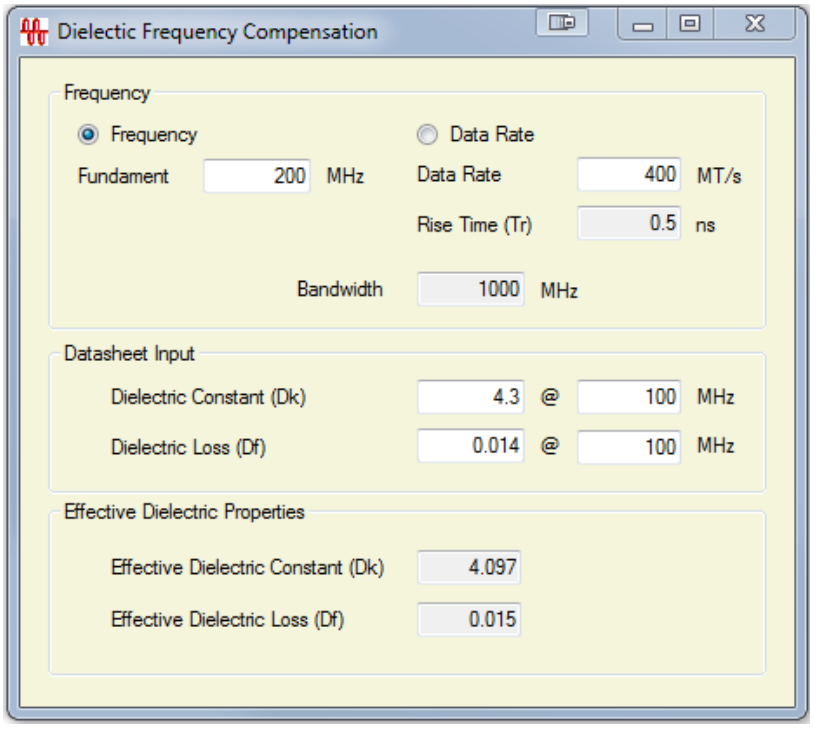

Figure 3 – Calculation of 'Effective' Dielectric Constant and Dielectric Loss

In Figure 3, a data rate of say 400MT/s or a fundamental frequency of 200MHz can be used to determine the maximum bandwidth. From that, the 'Effective' dielectric constant and loss can be

extrapolated. Unfortunately, most material datasheets specify the Dielectric Constant (Dk) and Dielectric Loss (Df) at 100MHz. This is the traditional test parameter however, that is now changing with the next generation of high-speed, low loss laminates that are specified up to 10GHz or more. Some low loss microwave materials are measured at 100GHz.

Typically for a digital design, a characteristic impedance of 50 - 60 ohms is used. But, this becomes more important as the edge rates become faster and also different technologies have their specific requirements. For example: Ethernet is 100 ohm and USB 90 ohms differential, DDR2 is 50/100 and DDR3/4 is 40/80 single ended/differential impedance. So controlling impedance with a number of different technologies can become a challenge. Also, as operating voltages are reduced, the associated noise margins are also reduced, making it even more important to match the impedance.

Stackup Planner | PDN Planner

2 Layer | 4 Layer | 6 Layer | 8 Layer | 10 Layer | 12 Layer | 14 Layer | 16 Layer | 18 Layer | 10L N4000-13

UNITS: mil — 4/3/2015 — Total Board Thickness: 65.32 mil

Differential Pairs > 50/100 Digital | 40/80 DDR3 | 90 USB

Layer No.	Via Span & Hole Diameter	Description	Layer Name	Material Type	Dielectric Constant	Dielectric Thickness	Copper Thickness	Trace Clearance	Trace Width	Current (Amps)	Characteristic Impedance (Zo)	Edge Coupled Differential (Zdiff)
		Soldermask		Liquid Photoimageable	4.0	0.5						
1	8 4 8	Signal	Top Layer	Conductive			1.38	10	7	0.46	41.75	79.92
		Prepreg		N4000-13; 106; Rc=75% (2.5GHz)	3.19	2.63						
2		Plane	GND_TOP	Conductive			0.71					
		Core		N4000-13 ; 106 ; Rc=68.3% (2.5GHz)	3.3	2						
3		Signal	MidLayer3	Conductive			0.71	6	4	0.19	42.97	80.76
		Prepreg		N4203-13EP; 2016; Rc=54% (2.5GHz)	3.60	4.67						
4		Signal	MidLayer4	Conductive			0.71	8	7	0.29	41.26	79.79
		Core		N4000-13 ; 1080/106 ; Rc=56.9% (2.5G...	3.6	4						
5		Plane	PWR_TOP	Conductive			0.71					

Figure 4 – Multiple differential pair technologies per substrate

Figure 4 illustrates the ICD Stackup Planner's unique differential pair calculation. In this case, digital, DDR3 and USB technologies are all accommodated on Nelco N4000-13, 2.5GHz material.

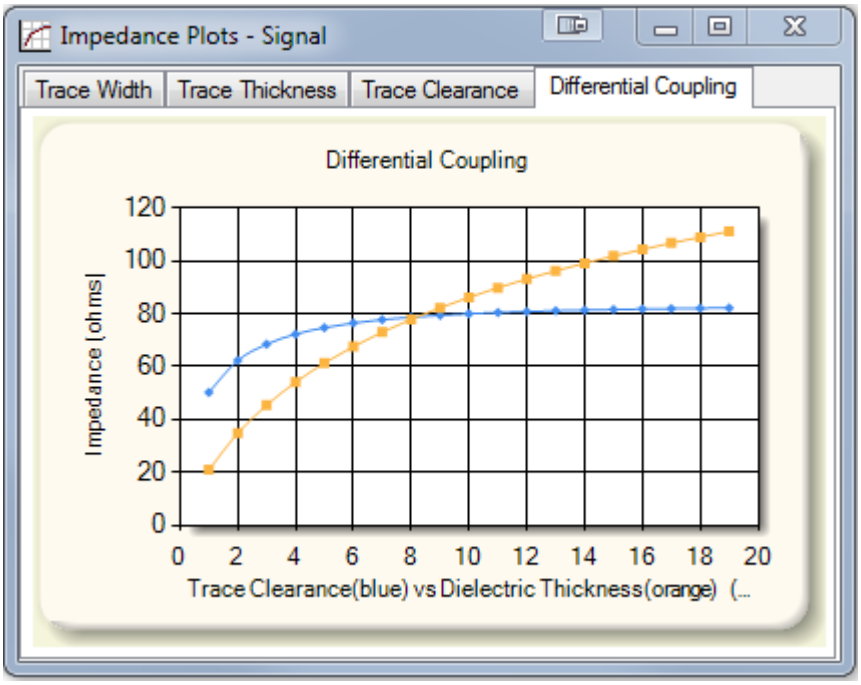

Figure 5 – Multiple field solver passes produce Differential Coupling plot

With differential impedance, there comes a (coupling) point whereby increasing the trace separation or the dielectric thickness has little or no further effect on impedance. At this point, the impedance

rolls off and the traces become uncoupled. This is also the point where crosstalk of unrelated signals begins to occur. For the microstrip stackup of Figure 4, Figure 5 shows this differential coupling point at 8mils. So, where I have a 10mil trace clearance for the 79.92 ohms differential impedance, I should have backed this off to just 8mil trace clearance in order to maintain sufficient coupling otherwise the two traces begin to act as individual single ended signals of 41.75 ohms.

For crosstalk, 8mils (in this case) is also the minimum separation before coupling occurs. This gives you a defined clearance rule, to constrain routing, in order to avoid edge coupled crosstalk of long parallel trace segments.

In conclusion, controlled impedance design is not just a matter of pushing a button to get the right trace width for the desired impedance. It is an interactive process of manipulating five variables in combination with the material your preferred fab shop stocks to achieve an educated result. Your product will not only be manufacturable but also exhibit improved signal quality, reduced crosstalk and electromagnetic radiation and also perform reliably over many years.

Points to Remember

- A good transmission line is one that has constant impedance along the entire length of the line.
- The impedance of the driver must match the transmission line to avoid reflections.
- Drivers do not have the exact impedance to match the line (typically 10 – 35 ohms).
- Impedance matching slows down the rise and fall times, reduces the ringing (over/under shoot) of clock drivers and enhances the signal quality of a high-speed design.
- Impedance plots are simulated by multiple passes of the field solver to create heads-up plots of how to adjust the particular variables to get the desired impedance.
- If you select too low an impedance, the di/dt will increase, drawing excessive current form the supply and no doubt, creating further power integrity issues.
- Controlling impedance is a trade-off between trace width, trace (copper) thickness, dielectric thickness, dielectric constant and trace clearance.
- The dielectric constant and loss of all materials varies with frequency.
- Multiple differential pair technologies should be accommadated on the same substrate.
- The coupling point is where increasing the trace separation or the dielectric thickness has little or no further effect on differential impedance. At this point, the impedance rolls off and the traces become uncoupled. This is also the point where crosstalk of unrelated signals begins to occur.

References

Beyond Design: Embedded Signal Routing – Barry Olney
Beyond Design: Impedance Matching – Barry Olney
Signal and Power integrity Simplified – Eric Bogatin
How and why of obtaining accurate impedance calculations – Lee Ritchie
For information on the ICD Stackup and PDN Planner, please go to www.icd.com.au

Bio:

Barry Olney is Managing Director of In-Circuit Design Pty Ltd (ICD), Australia. The company developed the ICD Stackup Planner and ICD PDN Planner software, is a PCB Design Service Bureau and specializes in board level simulation.

