

BOARD LEVEL SIMULATION SPECIALISTS

ICD Stackup Planner - offers engineers/PCB designers unprecedented simulation speed, ease of use and accuracy at an affordable price

- 2D (BEM) field solver precision
- Characteristic impedance, edge-coupled & broadside-coupled differential impedance
- Unique field solver computation of multiple differential technologies per stackup
- Heads-up impedance plots of signal and dielectric layers
- User defined dielectric materials library - over 16,250 materials up to 100GHz

ICD PDN Planner - analyze multiple power supplies to maintain low impedance over entire frequency range dramatically improving product performance

- Fast AC impedance analysis with plane resonance
- Definition of plane size/shape, dielectric constant & plane separation for each on-board power supply
- Extraction of plane data from the integrated Stackup Planner
- Definition of voltage regulator, bypass/decoupling capacitors, mounting loop inductance
- Frequency range up to 100GHz
- Extensive Capacitor Library – over 5,250 capacitors derived from SPICE models

Concurrent design cuts development cost and time

By Barry Olney, In-Circuit Design.

The traditional printed circuit board (PCB) design process is to execute each stage of the design in sequence. But, as designs become more complex and time-to-market schedules become more demanding, one must take advantage of pre-layout simulation and simultaneous process design in order to beat the competition.

The pressure is on engineering managers to achieve more with their existing resources, although the design tasks have become more complex with increased levels of functional integration.

Concurrent design is the practice of developing products in which the different stages run simultaneously, rather than consecutively. It lowers product development time as well as time to market, leading to improved productivity and reduced costs.

Concurrent design is a relatively new process strategy and, although the initial implementation can be challenging, the competitive advantage means it is beneficial in the long term. It eliminates the need to have multiple design iterations, by creating an environment for designing a product right, first time.

Typically, a high-speed computer based product takes two to three iterations to develop a working prototype. However, these days the product lifecycle is very short and therefore time to market is of the essence. A board iteration can be very costly, not only in engineering time, but also in the cost of delaying the product's market launch. This missed opportunity could cost hundreds of thousands of Rands.

All of these factors impact on company profit, by increasing prototype costs and time to market. Computer based products have a very small market window these days (e.g. one year). If the product is delayed by six months (e.g. two re-spins) then the company has lost half its projected return.

Figure 1 illustrates the traditional design process compared to the simultaneous (parallel) design process. Pre-layout simulation can be done during design capture to establish the required design constraints. Functional sections of previously developed 'golden' boards can be reused, giving high confidence in performance,

and multiple designers can be employed on the same layout. Post-layout simulation and mechanical integration can be done towards the end on the layout to ensure compliance to specification prior to fabrication. This process can dramatically reduce development time.

The significant business benefits of concurrent engineering make it a compelling strategy to adopt. Over and above reduced development time and cost, it results in earlier identification of design problems so that potential issues can be corrected sooner, rather than at a later stage in the development process.

Process improvement is a systematic approach to ensure a development team optimises its underlying processes to achieve more efficient results. Process improvement is an aspect of organisational development in which a series of actions are taken to identify, analyse and improve existing design processes to meet new goals and objectives, such as increasing profits and performance, reducing costs and accelerating schedules.

These actions often follow a specific methodology or strategy to increase the likelihood of successful results. There are many ways to improve efficiency in the PCB design process; the most important of these are explored below.

Simulation

Pre-layout analysis allows a designer to identify and eliminate signal integrity, crosstalk and EMI issues early in the design process. This is the most cost-effective way to design a board with fewer iterations, rather than starting with the 'find-and-fix' based post-layout simulation.

There are multiple facets to pre-layout analysis, including:

- Stackup planning for controlled impedance, SI, crosstalk and cost control.
- Dielectric material selection for manufacturing yield, and high-frequency operation.
- PDN optimisation for product reliability and cost reduction.
- I/O buffer and drive strength selection.
- Topology optimisation.
- Termination strategy.
- Floor planning for critical components.
- Deriving layout routing constraints, including trace width, spacing and length matching.
- Signal integrity analysis to meet the design specifications with respect to noise margins, timing, skew, crosstalk and signal distortion.

Although the trace impedance is specified on the fabrication drawing, stackup planning is often left until Gerbers are produced and the deliverables are sent off to the fab shop. However, generally the virtual dielectric material selection and trace width and clearance provided do not match the desired controlled impedance, so the CAM engineer returns the calculations that may require trace width and clearance changes. This is not what is needed at the end of the design cycle.

This flawed process can be attributed to the fact the PCB designers do not have access to field solvers during layout and either have to wait until an SI engineer analyses the design or – as commonly occurs – wait for the fab shop's report.

In-Circuit Design (ICD) has responded to this challenge by developing a bidirectional interface from the ICD Stackup Planner to Altium Designer 14. This new interface allows the designer to extract the rigid/flex stackup from the Altium Layer Stack Manager into the Stackup Planner.

High-speed materials (up to 40 GHz) can be merged from the dielectric materials library, consisting of over 8800 materials, and the impedance of multiple differential pairs can be simulated on the same substrate. Once finalised, the designer simply exports the data, including PTH and blind and buried microvia spans, trace width and clearances and differential pair rules back into Altium Designer. This allows the designer to route to impedance. A fabrication drawing of the stackup specifying all HDI requirements is also exported to Excel.

Similarly, PDN analysis is often overlooked completely. It cannot be stressed enough how important low AC impedance is for high-speed designs that demand high current drain at low core voltages. If the impedance is high at either the fundamental frequency or any of the odd harmonics, then higher levels of electromagnetic radiation can be expected. This has a

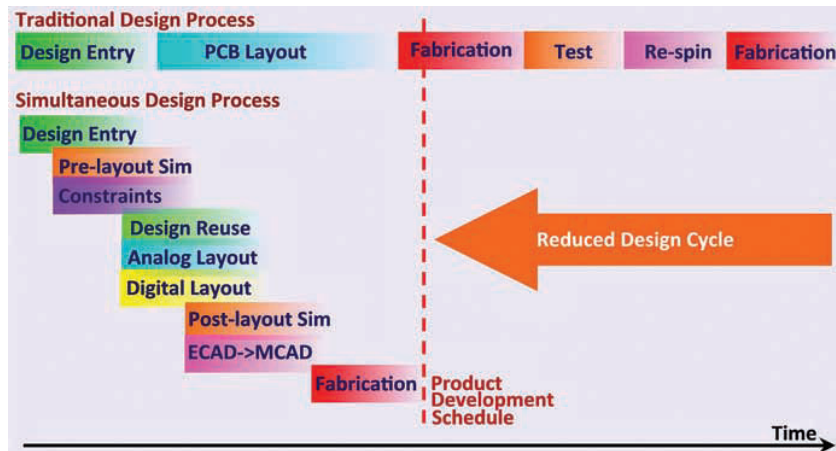


Figure 1. Traditional design process compared to the simultaneous design process.

direct impact on product reliability and the ability to meet electromagnetic compliance.

For years, application notes have recommended the use of three decoupling capacitors per power pin. This generally consisted of a 100 nF, 10 nF and a 47 pF capacitor. The idea behind this was that different values provided current at different frequencies, but unfortunately not the right frequencies as all boards are different.

As can be seen in Figure 3, multiple capacitors per decade are required to keep the effective impedance of the PDN below the target up to the required bandwidth. If too few capacitors are used, spread widely across the frequency domain, then there is a good chance that anti-resonance peaks in the PDN will exacerbate the problem.

Also, in this case, 3M Embedded Capacitance Material (ECM) has been incorporated, which is the only practical way to pull the PDN low around the GHz region. This material provides 3,1 nF/cm² which is an excellent way of amassing additional planar capacitance. The tight integration between ICD Stackup Planner and PDN Planner allows the automatic transfer of the effects of different dielectric materials to the PDN for analysis.

Design reuse

If the same switching regulator or processor and memory chips, for instance, are used on consecutive designs, creating a library of matching reuse blocks, or snippets, for schematic and PCB makes the best use of existing design elements for future designs. One can simply add a sub-circuit block to the schematic, transfer to the PCB database, and load a predefined layout block including component placement, tracks, copper and text.

Whether it is used for multiple channel designs, critical digital circuitry, RF circuit blocks, or just to replicate a commonly used layout pattern, design reuse will save time and ensure repeatability of design: a proven, tested, working solution to just drop into place.

Collaborative PCB design

For many years designers have attempted team design to avoid the seemingly unavoidable routing bottleneck, using multiple PCB designers to route different sections of the board at the same time. Schematics and layouts can be divided into function blocks, for example: power supply,



Figure 2. Integration of the ICD Stackup Planner and Altium Designer 14.

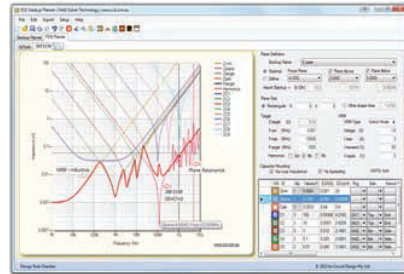


Figure 3. PDN analysis using multiple capacitors per decade and 3M ECM planar material.

analog, digital, memory and SERDES. Or, multiple designers can work on the same section simultaneously in different parts of the world.

Co-design implies that a group of designers can work on a design at the same time and all their design inputs are accepted. But, obviously, this is full of traps and there has to be some form of priority when merging databases.

In recent years some EDA companies have developed tools to enable designers to collaborate, compare and merge designs. These capabilities include the ability for multiple designers to access and merge a PCB database; a mechanism to accurately identify and compare databases; and the capacity to display the differences and allow the lead designer to select the best outcome of any conflicts.

Also, live collaboration is now possible. Each designer defines a work region and this is displayed clearly on each designer's database view, allowing them to avoid conflicts. Other tools allow designers to work with the one database in real time, with no need to partition and re-assemble the design. The tool manages edits from all users and continually sends updates to the entire team.

Team collaboration can result in extreme reductions in design time with a typical 13 week complex design being reduced to 5 weeks and in some cases providing a 60% increase in productivity.

Virtual prototyping – ECAD/MCAD collaboration

Like simulation, the integration of mechanical aspects of the design process is generally not considered until late in the design process. This leaves the design open to change once the mechanical issues have been identified – hence delay.

With stylish housings, how do designers fit the tightly packed, complex shaped electronics into the box? Traditionally, designers assumed there was no problem and simply handed over the CAD drawing to be manufactured. But after years of denial, it has been concluded that this approach did not work too well.

The challenges that many companies face, when they use both 2D and 3D design tools, is that these tools are fundamentally disconnected. The design that is created in 2D, in order to be reused in 3D, has to either be imported or recreated in the 3D tool. This disconnection causes inefficiencies in the design process. Also, any changes that are made in the 2D environment are not automatically reflected in 3D. This means that the user either has to go through the re-import process or create the change twice.

However, this issue has been overcome by some tools that bridge the gap between electronic and mechanical design to ensure that a product fits together every time. This is accomplished by using 3D DRC interference checking at the PCB design level and dynamically linking the 2D back into the 3D design space. This is a great solution to the problem – a native 3D environment.

In conclusion, concurrent design offers significant benefits to product development teams, providing a competitive advantage by reducing time to market and cost while providing high-performance, reliable products on time. Delivering a product on schedule provides higher returns due to a longer presence in the market. This all of course leads to higher profits.

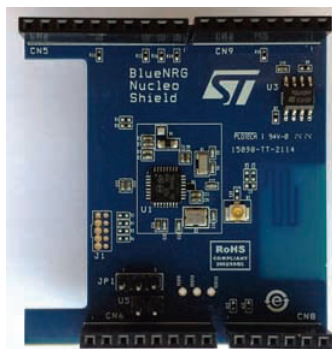
For more information contact EDA Technologies, +27 (0)12 665 0375, sales@edatech.co.za.

Bluetooth low energy evaluation board

The X-NUCLEO-IDB04A1 is a Bluetooth low energy (BTLE) evaluation board to allow expansion of the STM32 Nucleo boards from STMicroelectronics.

It is compatible with the Arduino UNO R3 connector layout, and is designed around BlueNRG, a Bluetooth low energy network coprocessor compliant with BTLE 4.0.

The new board interfaces with the



STM32 MCU via SPI, and the user can change the default SPI clock, the SPI chip select and SPI IRQ by changing one resistor on the board. A comprehensive, free development firmware library and example for BlueNRG, compatible with STM32Cube firmware, are provided.

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