

BOARD LEVEL SIMULATION SPECIALISTS

ICD Stackup Planner - offers engineers/PCB designers unprecedented simulation speed, ease of use and accuracy at an affordable price

- 2D (BEM) field solver precision
- Characteristic impedance, edge-coupled & broadside-coupled differential impedance
- Unique field solver computation of multiple differential technologies per stackup
- Heads-up impedance plots of signal and dielectric layers
- User defined dielectric materials library - over 16,250 materials up to 100GHz

ICD PDN Planner - analyze multiple power supplies to maintain low impedance over entire frequency range dramatically improving product performance

- Fast AC impedance analysis with plane resonance
- Definition of plane size/shape, dielectric constant & plane separation for each on-board power supply
- Extraction of plane data from the integrated Stackup Planner
- Definition of voltage regulator, bypass/decoupling capacitors, mounting loop inductance
- Frequency range up to 100GHz
- Extensive Capacitor Library – over 5,250 capacitors derived from SPICE models

Board Level Simulation

by Barry Olney | In-Circuit Design Pty Ltd | Australia

This article presents a brief overview of board level simulation for high-speed, multilayer design and highlights some common traps and some tips to hopefully get it right

Much has changed over the past 25 years that I have been involved in high-speed multilayer PCB design. Particularly, advances in lithography enables IC manufacturers to ship smaller and smaller dies on chips. In 1987 we thought that 0.5 micron technology was the ultimate but now days 28 nm technology is common. Also, power consumption, in FPGA's, has become a primary factor for FPGA selection. Whether the concern is absolute power consumption, usable performance, battery life, thermal challenges, or reliability, power consumption is at the centre of it all. In order to reduce power consumption, IC manufacturers have moved to lower core voltages and higher operating frequencies which of course means faster edge rates.

Faster edge rates mean reflections and signal quality problems. So even when the package hasn't changed and your clock speed hasn't changed a problem may exist for legacy designs. The enhancements in driver edge rates have a significant impact on signal quality, timing, crosstalk, and EMC. So whether you like it or – you are now a high-speed designer.

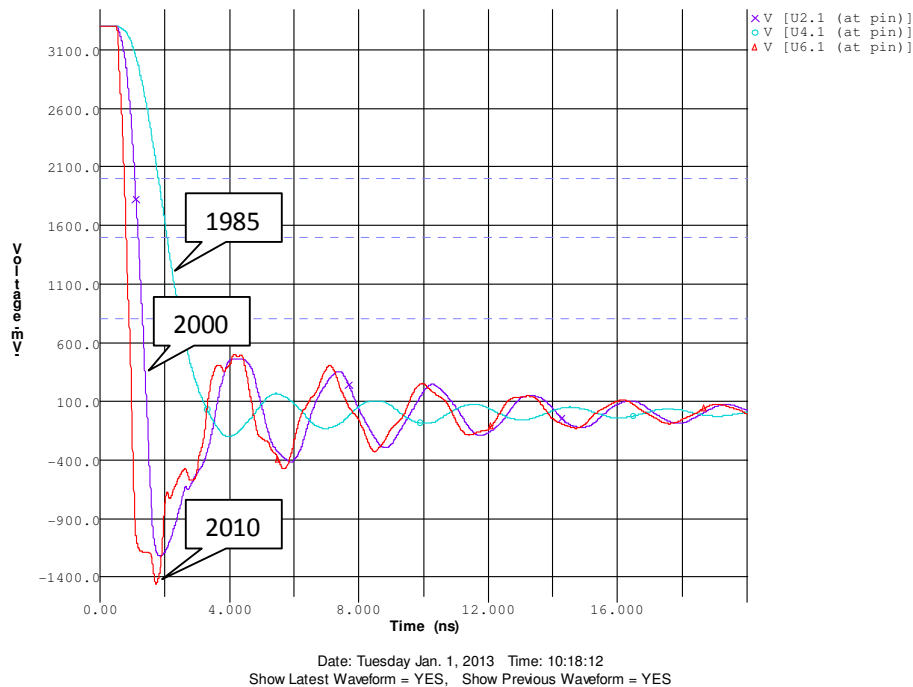


Figure 1. Edge rate changes over the past 25 years

Figure 1 illustrates the change in edge rates over the years – from 10ns back in 1985 to less than 1ns in 2010. The faster edge rate for the same frequency and same length trace creates ringing in the un-terminated transmission line. This also has a direct impact on radiated emissions. Figure 2 shows the massive increase in emissions from the slowest to fastest rise time. When dealing with 1ns rise times, the emissions can easily exceed the FCC/CISPR Class B limits for an un-terminated transmission line.

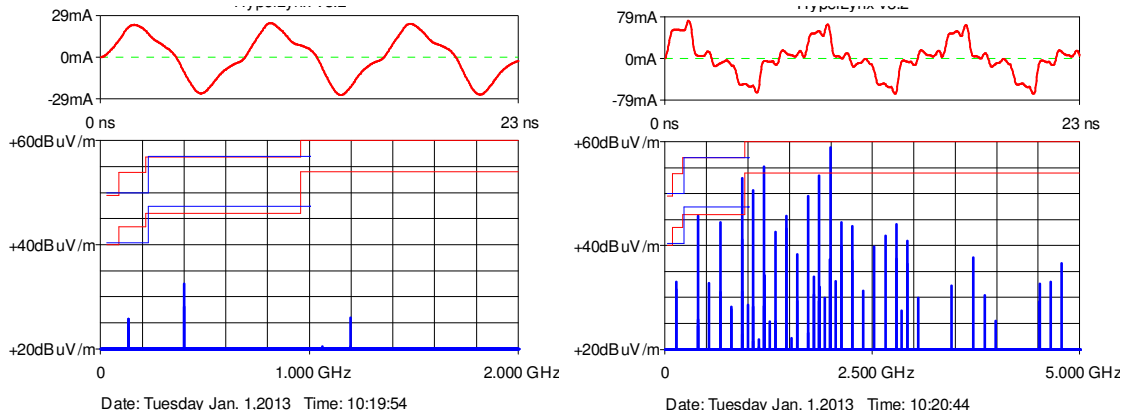


Figure 2. Radiated emissions from the 10 ns edge rate (left) and 1ns (right)

Also, today’s high-density, high-performance FPGA’s typically require a number of different power supplies (for example 3.3V, 2.5V, 1.8V and 1.5V) to power the core and I/O. These are best sourced from a switch mode power supply. Core current consumption depends upon utilization of the part (such as clock speed and internal elements used), but maximum values range from 1.5A to 10A. Current consumption for the I/Os depends on the voltage and the utilization of the I/O elements; however, for all I/O banks operating together, the maximum current demand can exceed 10A.

Another power management consideration that needs to be addressed is the monotonic rise of voltage in the core and I/O to their steady state levels. This consideration is critical for the correct operation of the FPGA because if the voltage sags during boot-up, the device may not reset. While many power supplies take this requirement into consideration, it is recommended to further support this requirement by the use of adequate bulk capacitance in the Power Distribution Network (PDN).

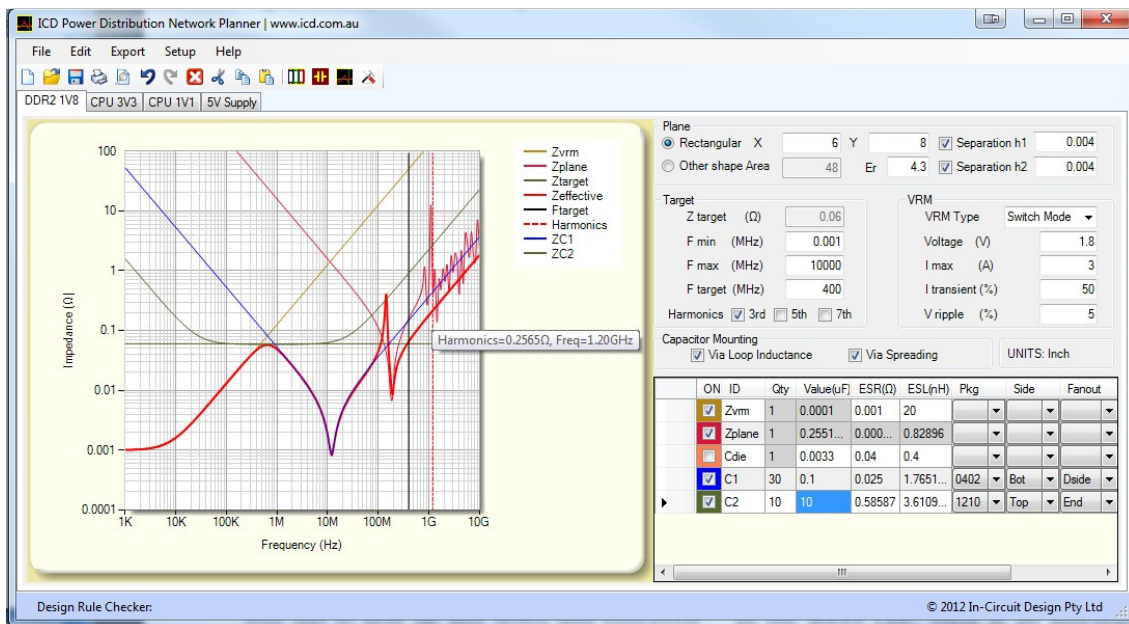


Figure 3. The PDN of a 1.8V DDR2 supply is analyzed by the ICD PDN Planner

Figure 3 illustrates the combined effect of the Voltage Regulator Module (VRM), 10μF bulk bypass, 100nF decoupling capacitors, the plane resonance of the board and capacitor mounting/loop

inductance for a typical DDR2, 1.8V supply. The objective is to keep the effective impedance as low as the target impedance (horizontal line) up to the fundamental frequency of the clock (400 MHz vertical line).

In the above case, there is an anti-resonance peak at 158 MHz, but fortunately that is well below the fundamental clock frequency of 400MHz. Also, one needs to keep the odd harmonics in mind. If the plane resonance appears at the 3rd (1.2GHz), 5th (2GHz) or 7th (2.8GHz) harmonic, there could be an issue. In this case, there is a peak at the 3rd harmonic so this needs to be addressed by changing the 1.8V plane size to reduce the resonance as the frequency approaches half wave length.

Apart from PDN planning, the board stackup integrity is the other issue that is most often overlooked when designing a high-speed board. The majority of designers leave the stackup planning to deal with at design completion – along with fabrication deliverables.

Also, before starting a PCB design, we need to plan the PCB stackup and ensure that the selected substrate materials are available from our chosen fabrication—a step that is regularly missed. Changing the stackup towards the end of the design process could mean changing trace widths and clearances to achieve the correct impedance, which could create a lot of unnecessary work.

If we use the same materials that the fab shop stocks to build our stackup, then the impedance will be more accurate. If we just choose a convenient number, for core thickness, for example, then this may be up to 3% different off from what is available; hence, the impedance will vary by 3%.

The most widely used dielectric material is FR4 and may be in the form of core or prepreg (pre-impregnated) material. Isola's top selling materials are FR406 and FR408. While FR406 sets the industry standard for basic multilayer PCB fabrication, FR408 is a high-performance FR4 epoxy dielectric for improved signal performance. Its low dielectric constant and low dissipation factor make it an ideal candidate for broadband circuit designs requiring fast signal speeds or improved signal integrity. Also, the high glass transition temperature makes it compatible with ROHS compliant components and most FR4 processes.

The configuration of the PCB Stackup depends on many factors but whatever the requirements one should ensure that the following rules are followed in order to avoid a possible debacle:

- All signal layers should be adjacent to and closely coupled to a reference plane, creating a clear return path and eliminating broadside crosstalk.
- There is good interplane capacitance to reduce inductance at high frequencies.
- High speed signals should be routed between the planes to reduce radiation.
- The substrate should be symmetrical with an even number of layers. This prevents the PCB from warping during manufacture and reflow.
- The stackup should accommodate a number of different technologies.
- Cost (the boss's most important design parameter) should also be addressed.

Figure 8 shows a typical 8 layer stackup that can be used for DDR2 and DDR3 designs. It is important to avoid adjacent layer crosstalk by having each signal in a stripline configuration between planes. Also, the high-speed signals should only be routed on these internal stripline layers to avoid microstrip radiation.

ICD Stackup Planner FX | Field Solver Technology | www.icd.com.au

File Edit Import Export Setup Help

2 Layer 4 Layer 6 Layer 8 Layer 10 Layer 12 Layer 14 Layer 16 Layer 18 Layer DDR3 8 Layer

ICD STACKUP PLANNER FX – www.icd.com.au 1/2/2013 Total Board Thickness: 58.4 mil

UNITS: mil

Differential Pairs > 50 ohm 100 ohm Diff 90 ohm USB

Layer No.	Description	Layer Name	Material Type	Dielectric Constant	Dielectric Thickness	Copper Thickness	Trace Clearance	Trace Width	Current (Amps)	Characteristic Impedance (Zo)	Edge Coupled Differential (Zdiff)	Broadside Coupled Differential (Zdbs)
	Soldermask		Dielectric	3.3	0.5							
1	Signal	Top	Conductive			1.4	8	4	0.31	53.9	100.34	
	Prepreg		Dielectric	4.3	3							
2	Plane	GND	Conductive			1.4						
	Core		Dielectric	4.3	8							
3	Signal	Inner 3	Conductive			1.4	14	6	0.42	52.34	99.32	
	Prepreg		Dielectric	4.3	12							
4	Plane	VCC	Conductive			1.4						
	Core		Dielectric	4.3	4							
5	Plane	GND	Conductive			1.4						
	Prepreg		Dielectric	4.3	12							
6	Signal	Inner 6	Conductive			1.4	8	6	0.42	52.09	90.24	
	Core		Dielectric	4.3	8							
7	Plane	VDD	Conductive			1.4						
	Prepreg		Dielectric	4.3	3							
8	Signal	Bottom	Conductive			1.4	8	4	0.31	53.9	100.33	
	Soldermask		Dielectric	3.3	0.5							

Design Rule Checker: © 2012 In-Circuit Design Pty Ltd

Figure 4. A typical 8 layer stackup simulated by the ICD Stackup Planner

I previously mentioned that it is important to keep the AC impedance of the PDN as low as possible. Decoupling and bypass capacitors are only effective up to about 400MHz. So to provide suppression at higher frequencies we need to use interplane capacitance. This is achieved by using a thin dielectric between the central power planes.

The power to ground plane capacitance provides an ideal capacitor in that it has no series lead inductance and no equivalent series resistance (ESR), which helps reduce noise at extremely high frequencies. Good interplane capacitance can be achieved by using 4-MIL plane spacing resulting in 241 pF/in². The higher the better. Whereas, 10-MIL spacing will only achieve 96.75 pF/in² and 60 MIL a dismal 16 pF/in².

Now that the two basic but most important part of the design is planned – the PDN and the stackup a pre-layout analysis is performed to establish placement and routing rules.

Flight time delay and skew are key pillars in high speed PCB design signal integrity. One of the driving factors for flight time and skew performance is the placement of components. Maximum placement refers to the placement in which the distances between the devices are the maximum distance permitted. Controlling the maximum placement of devices, combined with the assumption that good general design practices are adhered to, limits maximum trace delay to roughly the longest Manhattan distance of the signals contained in a specific clock domain.

Why the longest Manhattan distance? This is due to skew matching requirements: All of the shorter nets in a clock domain must be lengthened to skew match to the longest run length. Therefore, flight time and skew—for an entire clock domain—are governed by the maximum placement, along with the routing rules that constrain the matching of the trace lengths.

In the classic high-speed design flow, timing specifications simulation results are compared to determine placement and routing constraints. Given a length constraint, a designer can control signal integrity by controlling the PCB trace topology of the various parts of an interface. Included in this topology are any terminations.

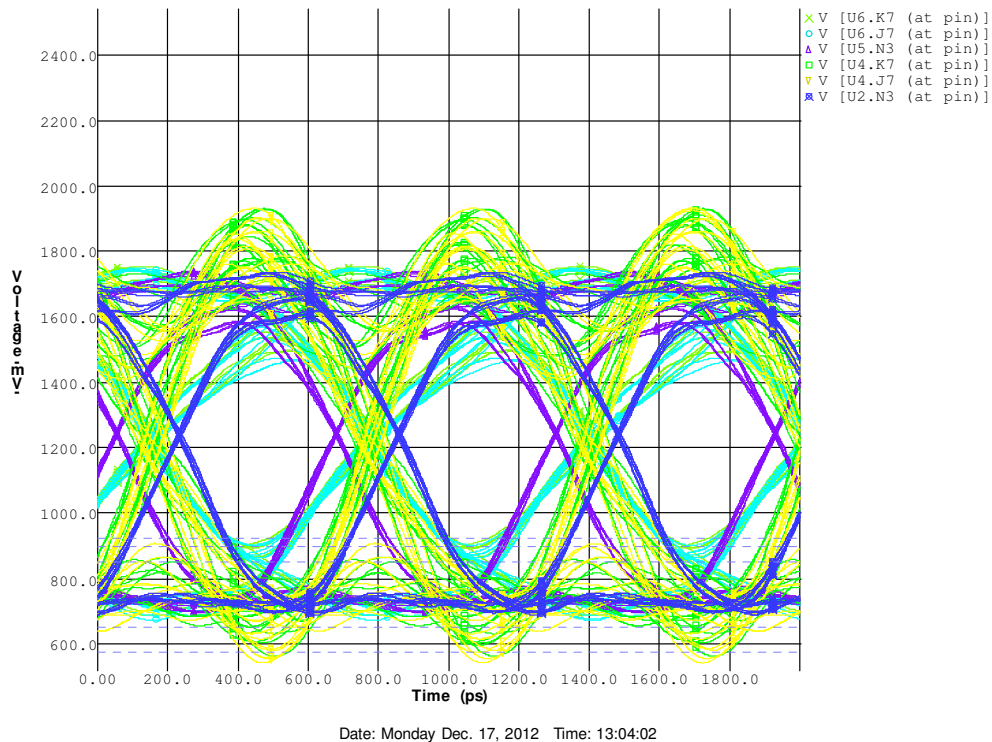


Figure 5. Skew of clock to address, control and command signals of DDR3 memory

Figure 5 illustrates the timing of the clock compared to the address, control and command signals of a DDR3 memory design. Also, the skew between data lanes and data strobes should be kept to a minimum and the eyes should be wide open. DDR3 is much easier to route, in fact, than DDR2 as leveling can be used to synchronize the delay of data lanes.

Unfortunately, board-level simulation is engaged too often towards the end of the design cycle. Ideally, the simulation should be done during the design process or even better still – before a single chip is placed on the board, to ensure design integrity.

A preliminary batch mode simulation is first completed on the design. Default IC characteristics, crosstalk of 150mV maximum and EMC to FCC, CISPR Class A and B are setup in the simulator. The batch mode simulation automatically scans large numbers of nets on an entire PCB, flagging Signal Integrity, Crosstalk and EMC hot spots.

The post-layout simulation analysis can then be prepared using supplied specifications. This report contains the results of the extensive Interactive Board Level Simulation which takes the analysis to the next level - simulating trouble spots identified by the batch analysis in order to further resolve the issues with greater accuracy.

The critical signals are again checked now that the physical information is obtained from the PCB data base (eg trace lengths, clearances, vias etc) to ensure that the design complies to specification. Figure 6 measures the DQ0 signal at the load.

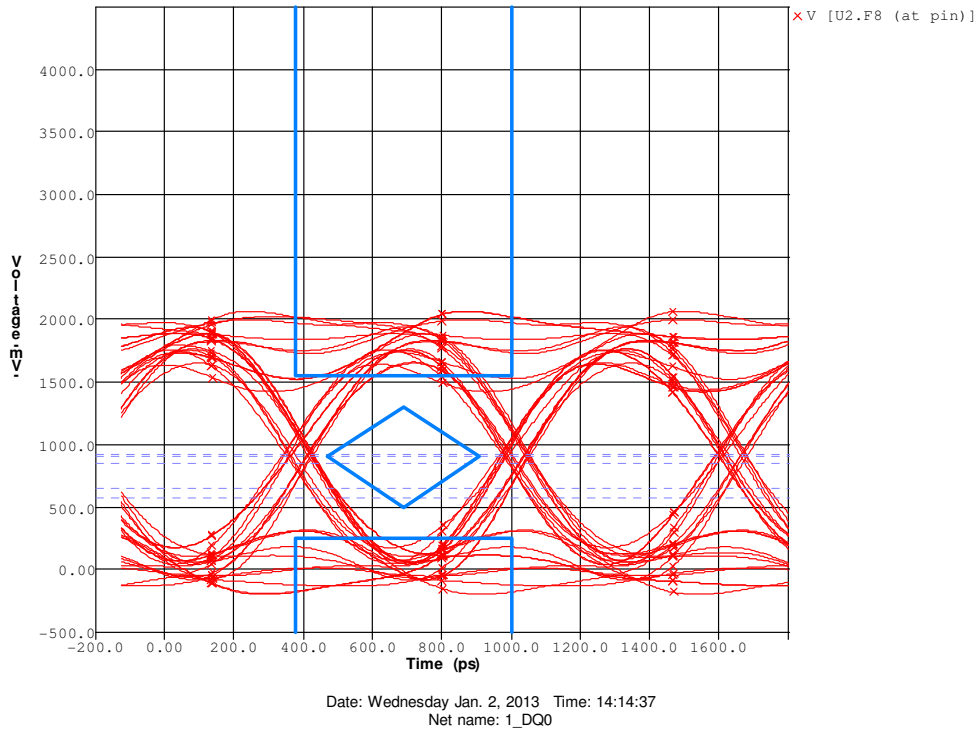


Figure 6 measures the DQ0 waveform at the load.

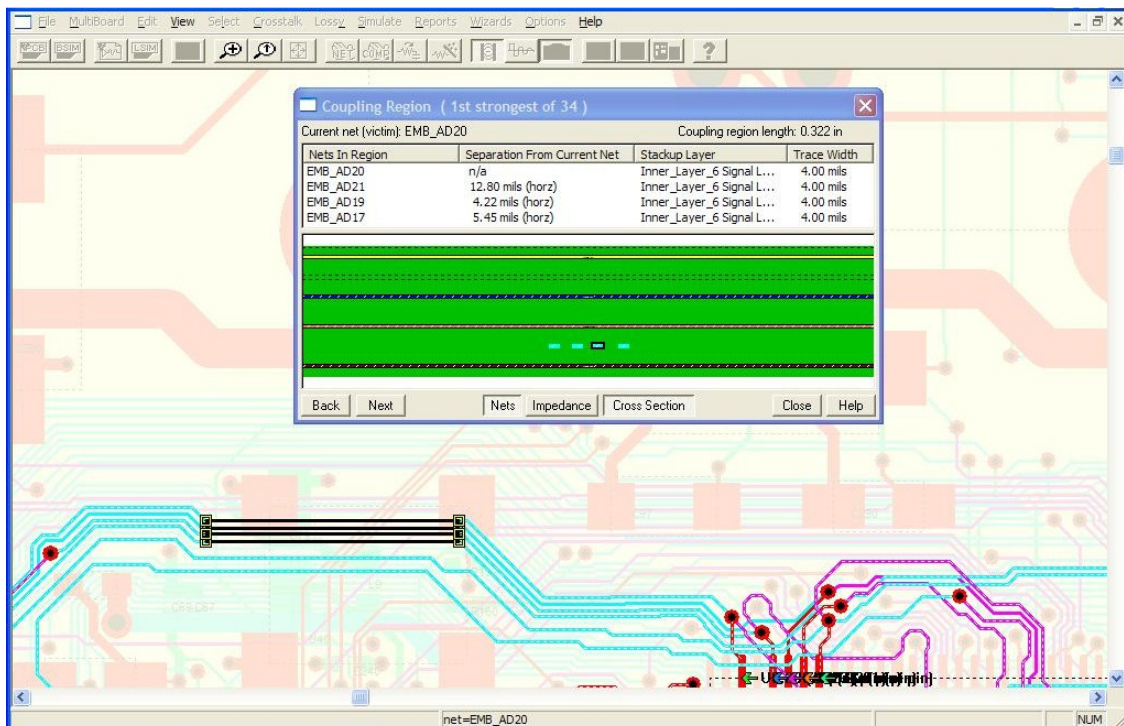


Figure 7 Crosstalk on long parallel trace segments

Crosstalk is typically picked up on long parallel trace segments. These can be on the same layer as in Figure 7 but may also be broadside coupled from the adjacent layer. It is for this reason that

orthogonal routing is recommended on adjacent layers (between planes) to minimize the coupling area. This will not occur with the stackup illustrated in Figure 4, because there is only one signal layer between the planes – so this is very safe as far as broadside crosstalk is concerned.

High-speed boards can be designed to work right the first time, with little additional effort, providing you follow a tried and proven process that results in a reliable, manufacturable design that conforms to specifications and is produced on time and to budget.

We all know that simulation tools aren't cheap and then there is a learning curve associated with complex software not to mention that the Engineer needs to have years of experience analyzing high speed designs. By utilizing a PCB Board Level Simulation Service, you can be assured that your PCB will be reliable, manufactureable, conforms to specifications and passes the relevant compliancy tests saving you time, money and frustration for a fraction of the cost of board iterations and multiple compliancy testing. Plus, the simulation can be done before the design is finalized (before Gerber output or even earlier in the design process) to further reduce production time and costs.

References:

Advanced Design for SMT – Barry Olney

Intro to Board-Level Simulation and the PCB Design Process – Barry Olney

PCB Design Techniques for DDR, DDR2 & DDR3, Part 1 & 2 – Barry Olney

The ICD Stackup and PDN Planner can be downloaded from www.icd.com.au

Bio -

Barry Olney is Managing Director of In-Circuit Design Pty Ltd (ICD), Australia. The company develops the ICD Stackup Planner and ICD PDN Planner software, is a PCB Design Service Bureau and specializes in board level simulation.

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