

BOARD LEVEL SIMULATION SPECIALISTS

ICD Stackup Planner - offers engineers/PCB designers unprecedented simulation speed, ease of use and accuracy at an affordable price

- 2D (BEM) field solver precision
- Characteristic impedance, edge-coupled & broadside-coupled differential impedance
- Unique field solver computation of multiple differential technologies per stackup
- Heads-up impedance plots of signal and dielectric layers
- User defined dielectric materials library - over 16,250 materials up to 100GHz

ICD PDN Planner - analyze multiple power supplies to maintain low impedance over entire frequency range dramatically improving product performance

- Fast AC impedance analysis with plane resonance
- Definition of plane size/shape, dielectric constant & plane separation for each on-board power supply
- Extraction of plane data from the integrated Stackup Planner
- Definition of voltage regulator, bypass/decoupling capacitors, mounting loop inductance
- Frequency range up to 100GHz
- Extensive Capacitor Library – over 5,250 capacitors derived from SPICE models

Beyond co-design

As designs become more complex and time-to-market schedules become more demanding, engineers must take advantage of pre-layout simulation and simultaneous process design in order to beat the competition. By Barry Olney, CEO, In-Circuit Design Pty Ltd

Concurrent design can decrease product development time and also the time-to-market, leading to improved productivity and reduced costs. As a relatively new process strategy, initial implementation can be challenging but the potential competitive advantage means it is beneficial in the long term. Typically, a high-speed computer based product takes two to three iterations to develop a working prototype. However, these days the product life cycle is very short and therefore time-to-market is of the essence. A board iteration can be very costly, not only in engineering time, but also in the cost of delaying the product's market launch. This missed opportunity could cost hundreds of thousands of dollars. All of the above impact on

company profit, by increasing prototype costs and the time-to-market.

In a concurrent approach, pre-layout simulation can be done during design capture to establish the required design constraints. Functional sections of previously developed 'golden' boards can be reused giving high confidence in performance and multiple designers can be employed on the same layout. Post-layout simulation and mechanical integration can be done towards the end on the layout to ensure compliance to specification prior to fabrication. This process can dramatically reduce development time.

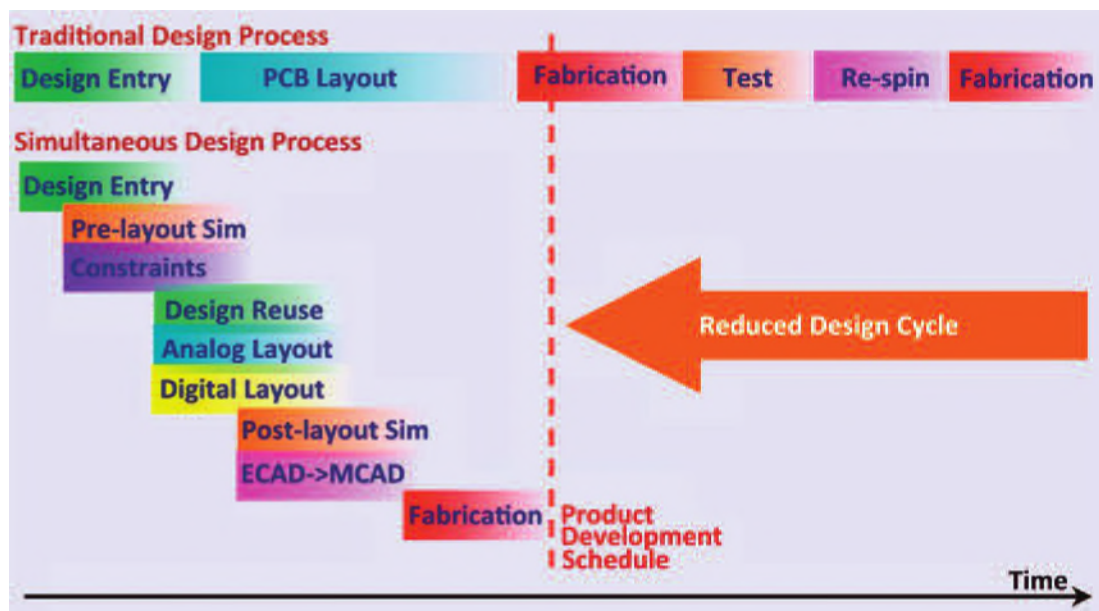
Process improvement is a systematic approach to ensure a development team optimises its underlying processes to achieve more efficient results. Process improvement is an aspect of organisational development in which a series of actions are taken to identify, analyse and improve existing design processes to meet new goals and objectives, such as increasing profits and performance, reducing costs and accelerating

schedules. These actions often follow a specific methodology or strategy to increase the likelihood of successful results. There are many ways to improve efficiency in the PCB design process, such as: simulation; design reuse; collaborative PCB Design, and virtual Prototyping.

Simulation

Pre-layout analysis allows a designer to identify and eliminate signal integrity,

Figure 1: A traditional design process compared to the simultaneous, or concurrent, design process



crosstalk and EMI issues early in the design process. This is the most cost effective way to design a board with fewer iterations, rather than starting with the 'find-and-fix' based post-layout simulation. There are multiple facets to pre-layout analysis including: stackup planning for controlled impedance, SI, crosstalk, and cost control; dielectric material selection for manufacturing yield, and high-frequency operation; PDN optimisation for product reliability and cost reduction; I/O buffer and drive strength selection; topology optimisation; termination strategy; floor planning for critical components; deriving layout routing constraints, including trace width, spacing and length matching, and signal integrity analysis to meet the design specifications with respect to noise margins, timing, skew, crosstalk, and signal distortion.

Although the trace impedance is specified on the fabrication drawing, stackup planning is often left until Gerber's are produced and the deliverables are sent off to the Fab shop. However, generally the virtual dielectric material selection and trace width and clearance provided do not match the desired controlled impedance. So, the CAM engineer returns the calculations that may require trace width and clearance changes; not what is needed at the end of the design cycle. This flawed process can be attributed to the fact that PCB Designers do not have access to field solvers during layout and either have to wait until an SI Engineer analyses the design or, as commonly occurs, wait for the Fab shop's report.

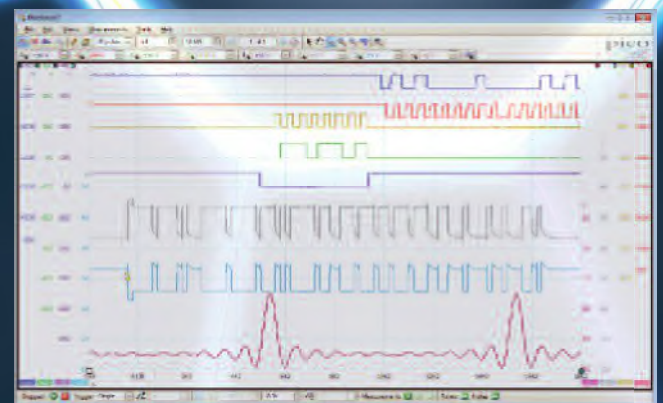
ICD has responded to this challenge by developing a bi-directional interface from the ICD Stackup Planner to Altium Designer 14. This new interface allows the designer to exact the rigid/flex stackup from the Altium, Layer Stack Manager into the Stackup Planner. High-speed materials (up to 40GHz) can be merged from the Dielectrics Materials Library, of over 8,800 materials, and the impedance of multiple differential pairs can be simulated on the same substrate. Once finalised, the designer simply exports the data, including PTH and blind and buried microvia spans, trace width and clearances and differential pair rules

pico[®]
Technology

8 CHANNEL PC OSCILLOSCOPE

For just £1395 €1689 \$2302

- High resolution
- USB powered
- Deep memory



INCLUDES AUTOMATIC MEASUREMENTS,
SPECTRUM ANALYZER, SDK, ADVANCED TRIGGERS,
COLOR PERSISTENCE, SERIAL DECODING (CAN, LIN, RS232,
I²C, I²S, FLEXRAY, SPI), MASKS, MATH CHANNELS, ALL AS
STANDARD, WITH FREE UPDATES

12 bit • 20 MHz • 80 MS/s
256 MS buffer • 14 bit AWG

www.picotech.com/PS425

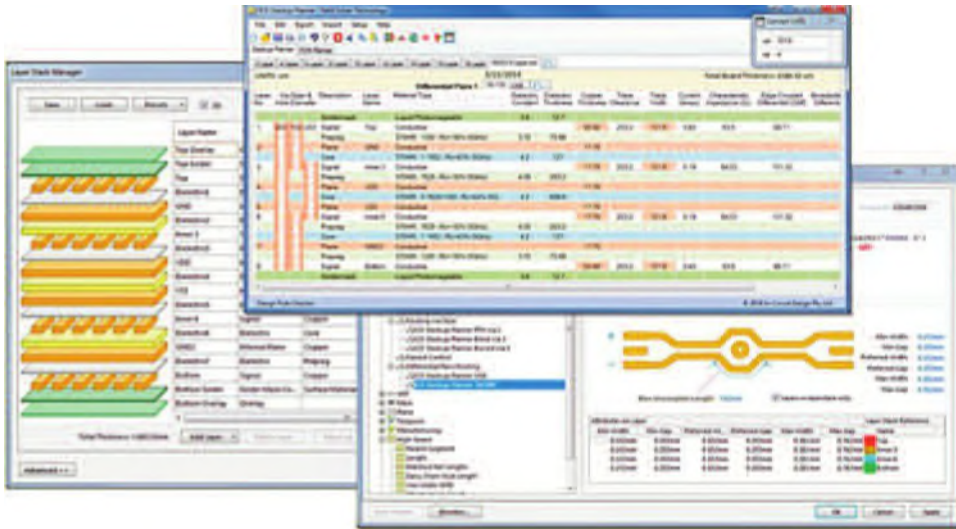


Figure 2:
Integration of the
ICD Stackup
Planner and Altium
Designer 14

back into Altium Designer. This allows the designer to route to impedance. A fabrication drawing of the stackup specifying all HDI requirements is also exported to Excel.

Similarly, PDN Analysis is often overlooked completely. It can't be overstressed how important low AC impedance is for high-speed designs that demand high current drain at low core voltages. If the impedance is high at either the fundamental frequency, or any of the odd harmonics, then higher levels of electromagnetic radiation can be expected. This has a direct impact on product reliability and the ability to pass Electromagnet Compliance.

For years, application notes have recommended the use of three decoupling capacitors per power pin. This generally consisted of a 100nF, 10nF and a 47pF capacitor. The idea behind this was that different values provided current at different frequencies, but unfortunately not the right frequencies as all boards are different. As can be seen in Figure 3, multiple capacitors per decade are required to keep the effective impedance of the PDN below the target up to the required bandwidth. If too few capacitors are used, spread widely across the frequency domain, then there is a good chance that anti-resonance peaks in the PDN will exacerbate the problem.

Also, in this case, the use of 3M Embedded Capacitance Material (ECM) has been incorporated, which is the only practical way to

pull the PDN low around the GHz region. This material provides 20nF/in² which is an excellent way of amassing additional planar capacitance. The tight integration between the ICD Stackup Planner and PDN Planner allows the automatic transfer of the effects of different dielectric materials to the PDN for analysis.

Further efficiency gains

If the same switching regulator or processor and memory chips, for instance, are used on consecutive designs, creating a library of matching 'reuse blocks or snippets' for schematic and PCB makes the best use of existing design elements for future designs. Simply add a sub-circuit block to the schematic, transfer to the PCB database, and load a predefined layout block including component placement, tracks, copper and text. Whether it is used for multiple channel designs, critical digital circuitry, RF circuit blocks, or just to replicate a commonly used layout pattern, design reuse will save time and ensure repeatability of design: a proven, tested, working solution to just drop into place.

For many years designers have attempted team design, to avoid the seemingly unavoidable routing bottleneck, using multiple PCB designers to route different sections of the board at the same time.

Schematics and layouts can be divided into function blocks for example: Power Supply, Analog, Digital, Memory and SERDES. Or, multiple designers can work on the same section simultaneously in different parts of the world. I have done this many times, providing an over-night design service for US based companies. Co-design implies that a group of designers can work on a design at the same time and all their design inputs are accepted. But obviously, this is full of traps and there has to be some form of priority when merging databases.

