

# Alternative Series Termination Techniques

## Beyond Design

by Barry Olney, IN-CIRCUIT DESIGN PTY LTD / AUSTRALIA

In a previous column on “[Transmission Line Terminations](#),” I discussed the three most common termination strategies: series, end, and differential. These techniques are used to eliminate impedance mismatch and hence reflections to avoid crosstalk and electromagnetic radiation. As a general rule, transmission line (trace) termination is necessary when the round trip propagation time of the signal is equal to or greater than the transition (rise or fall) time of the driver; otherwise, there will be data errors caused by signal degradation. In this month’s column, I will elaborate on two particular cases of series termination that every PCB designer will come across.

### 1. Distributing a Clock to Multiple Loads

The objective of the clock is to provide circuit timing and thereby coordinate the activity within the system. With memory circuits, the clock pulse will trigger the input and output of

data, and therefore, must be timed such that each bit of data arrives and stabilizes before the next clock cycle. To do this means that both the clock and data lines must be routed to exact delays within the specified setup and hold times. Since digital signals cannot be sped up, the only option is to add length to the line to delay the signal arrival to match the arrival speed of the longest lines in the bus. However, the clock signal should always be the longest delay of all so that the data signals have time to settle before they are clocked.

Routing clock signals to multiple loads can be done in many ways. A buffer could be used for each individual receiver, or the use of a dedicated clock driver incorporating a phase-locked loop (PPL) to synchronize the timing is also a common solution. However, this adds to the cost and consumes precious real estate.

Star routing is ideal for distributing a clock to multiple loads in low- to medium-speed

designs. The routing fans out from the driver through a series resistor for each load. This reduces reflections. The delay for each leg is then matched for each load. For clock lines with multiple receivers, it is best to route to the receiver that is the farthest from the driver first, and then match that delay when routing to the other receivers.

Clock signals generally have a fast rise time and hence are noisy due to high harmonic content; as a result, they must be isolated from the rest of the circuitry. To reduce the impact of a noisy clock circuit, it is good practice to locate the clock circuitry in the center of the PCB and star route out to the loads in precise patterns and at a specific delay.

The electromagnetic fields surrounding a microstrip (outer layer) trace exist partially within the dielectric material(s) and partially within the surrounding air. Since air has a dielectric constant of one, which is always lower than that of FR-4 and solder mask (typically 4.3 and 3.3, respectively), mixing a little air into the equation will lower the effective

dielectric constant and speed up the signal propagation. Even if the trace widths are adjusted on each layer, as the impedance is identical, the propagation speed of microstrip is always faster than stripline—typically by 13–17%.

The speed of propagation of digital signals is independent of trace geometry and impedance but reliant on the dielectric constant of the materials. Therefore, if a signal changes layers in the stackup, then the delay will also vary. If you are aware of this issue, then the trace delays (Figure 1) can be matched to compensate for the varying flight time so that at the nominal temperature, all signals running on either microstrip or stripline will arrive at the receiver simultaneously. PCB designers should always match delays—not length.

Before starting placement and routing, detailed interconnect routing constraints should be established. These constraints—based on pre-layout simulation, manufacturing restrictions, and IC manufacturer’s recommendations and guidelines—will control the place-

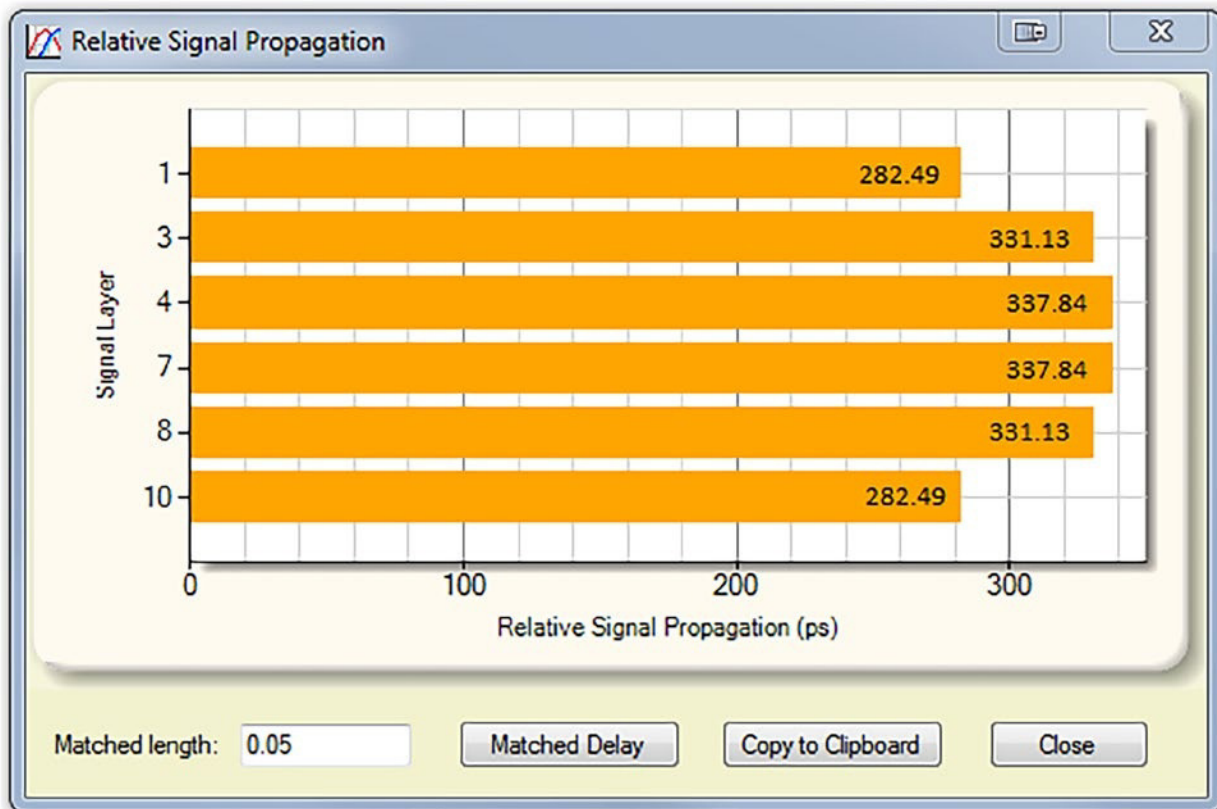


Figure 1: Relative signal propagation of microstrip and stripline (simulated in iCD Design Integrity).

ment and routing processes. Online design rule checks (DRCs) will warn the designer when a constraint is violated.

On a multilayer PCB, clock signals should be routed on a stripline (inner layer) sandwiched between two solid reference planes to reduce radiation. The spacing between the signal trace and the return planes should be as small as possible to increase coupling and reduce the loop area.

The three constraints to keep in mind include:

1. Route clock signals between the planes, fanout out close to the driver (200 mils) dropping to an inner layer, and route back up to the load again with a short fanout. A series terminator is required for each load.
2. Use the same reference plane (GND if possible) for the return signal, as this reduces the loop area and hence radiation.
3. Minimize crosstalk to other signals by keeping a distance of at least three times the trace width to sensitive signals.

## 2. Bi-Directional Data Termination

With series termination, the resistor needs to be close to the source (Figure 2). This ensures

that the reflected pulse sees the internal driver source impedance and the resistor in series (usually totaling 50 ohms). Since this matches the transmission line, it completely absorbs the reflected energy. However, data flows in both directions from the CPU to the memory, when writing to memory, then back from the memory to the CPU for reading the memory data. Where do we place the series terminator in a point-to-point configuration—at one end of the data-trace, or maybe in the center?

Out of habit—or perhaps for fear of doing the wrong thing—one would usually put the termination close to the CPU rather than the load. The simulated waveforms of the impact of having a termination resistor close to the driver, close to the load, and also in the middle of the transmission line show little distinction. However, there is a better unconventional solution: placing a termination resistor at each end of the transmission line (Figure 3). Figure 4 presents an improved eye diagram using this solution for both the read/write cycles.

Having a resistor at both ends of the transmission line, close to the driver and load, is an elegant solution as the resistor and input

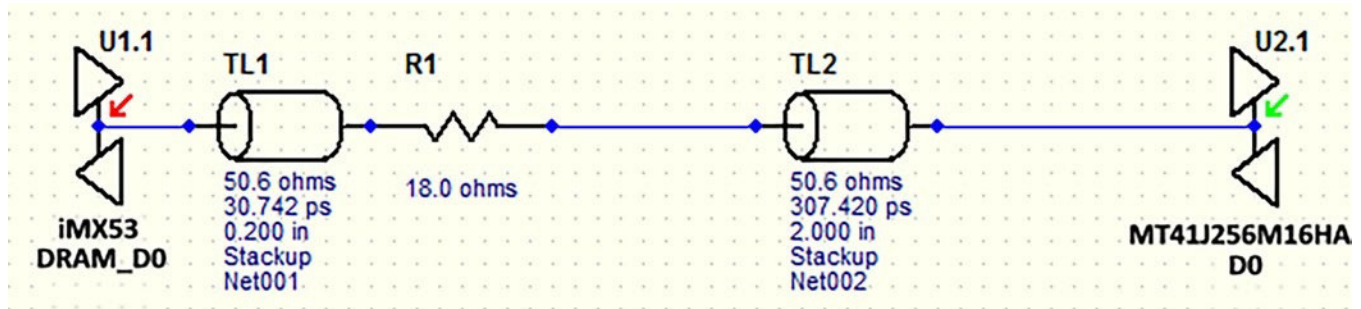


Figure 2: Typical series termination with a resistor close to the driver.

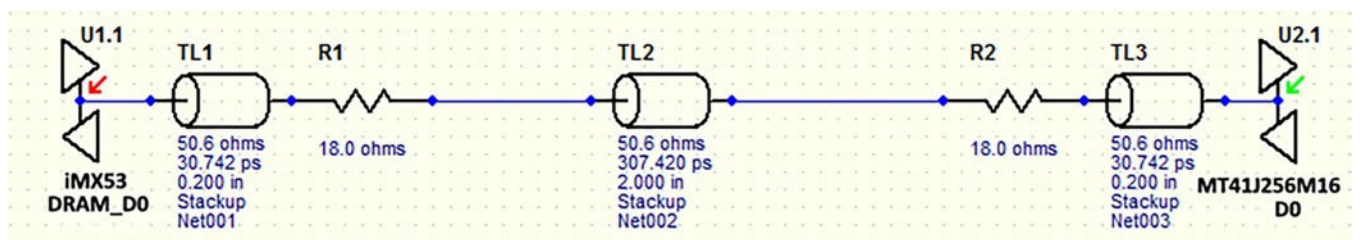


Figure 3: Series terminations at both ends (simulated in HyperLynx).

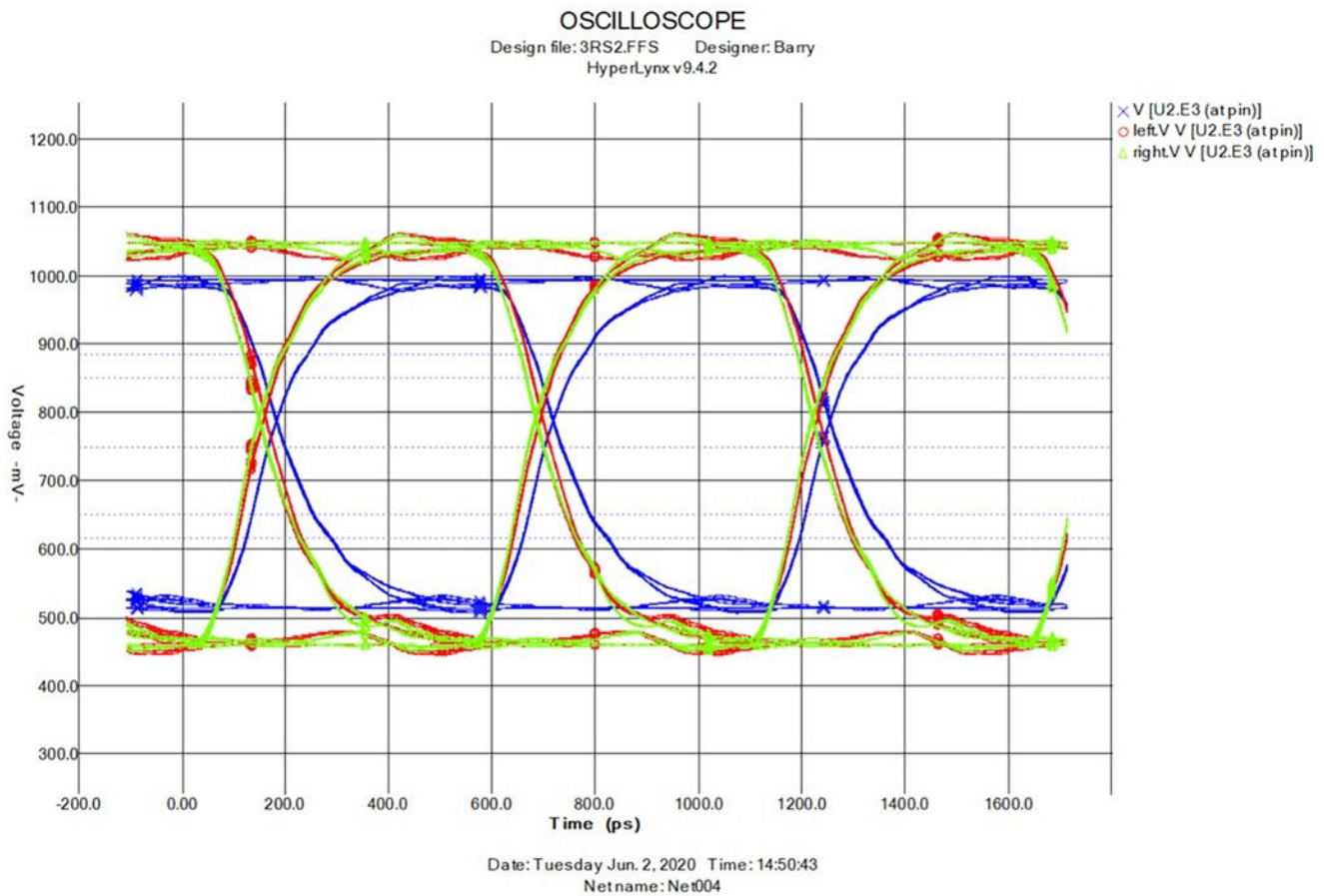


Figure 4: Comparison of the termination of both ends (blue) vs. the termination at either end.

capacitance of the tri-state load basically form an AC termination reducing reflections.

On-die termination (ODT) is implemented with several combinations of resistors on the later versions of DDR memory. Designers can use a combination of transistors which have different values of turn-on resistance. In the case of DDR2, there are three kinds of internal resistors: 150-ohm, 75-ohm, and 50-ohm. The internal on-die termination values in DDR3 are 120 ohms, 60 ohms, 40 ohms, and so forth. But for devices that do not incorporate ODT, dual-series terminations suffice.

### Key Points

- The three most common termination strategies are series, end, and differential.
- Transmission line termination is necessary when the round trip propagation time of the signal is equal to or greater than the transition (rise or fall) time of the driver.

- The objective of the clock is to provide circuit timing and thereby coordinate the activity within the system.
- For clock lines with multiple receivers, it is best to route to the receiver that is the farthest away from the driver first, and then match that delay when routing to the other receivers.
- The clock signal should have the longest delay of all so that the data signals have time to settle before they are clocked.
- Star routing is ideal for distributing a clock to multiple loads in low- to medium-speed designs.
- Clock signals generally have a fast rise time and hence are noisy due to high harmonic content; as a result, they must be isolated from the rest of the circuitry.
- The propagation speed of microstrip is always faster than stripline.

- The speed of propagation of digital signals is independent of trace geometry and impedance.
- PCB designers should always match delays—not length.
- Clock signals should be routed on a stripline (inner layer) sandwiched between two solid reference planes to reduce radiation.
- Placing a resistor at both ends of the transmission line, close to the driver and load, is an elegant solution to terminate a bi-directional signal. **DESIGN007**

### Further Reading

- B. Olney, "Beyond Design: Transmission Line Termination," *Design007 Magazine*, March 2020.
- B. Olney, "Beyond Design: The 10 Fundamental Rules of HSD Part 4," *Design007 Magazine*, December 2018.

- B. Olney, "Beyond Design: Signal Flight Time Variance in Multilayer PCBs," *The PCB Design Magazine*, December 2017.
- B. Olney, "Beyond Design: Effective Routing of Multiple Loads," *The PCB Design Magazine*, February 2014.
- Cadence Design Systems, "Contamination Delay in Clock Circuits: Best PCB Routing Techniques," February 24, 2020.
- H. W. Johnson & M. Graham, *High-Speed Digital Design: A Handbook of Black Magic*, Prentice-Hall, 1993.



**Barry Olney** is managing director of In-Circuit Design Pty Ltd (iCD), Australia, a PCB design service bureau that specializes in board-level simulation. The company developed the iCD Design Integrity software incorporating the iCD Stackup, PDN, and CPW Planner. The software can be downloaded at [icd.com.au](http://icd.com.au). To read past columns or contact Olney, [click here](#).

## Samsung-Accelerated Startup Luple Launches Devices to Balance Circadian Rhythms

Olly, a light technology device from Samsung's startup incubator, launched on Kickstarter and reached its funding goal in just 3 hours. The product is dedicated to helping users find balance in their everyday routines and comes

in two versions—Olly Day, which helps users stay awake during the day, and Olly Night, which encourages deeper and more holistic sleep at night.

Olly Day's wavelengths mimic sunlight to keep users feeling energized and to provide a natural energy boost without the side effects commonly associated with caffeine. The device boosts focus in just 20 minutes and can work more effectively and quickly than a cup of espresso.

Unlike LED lights that suppress the natural production of melatonin in the body, Olly Night's wavelengths encourage melatonin production to prepare users for a night's rest. The device emits a warm light and automatically turns off in 30 minutes.

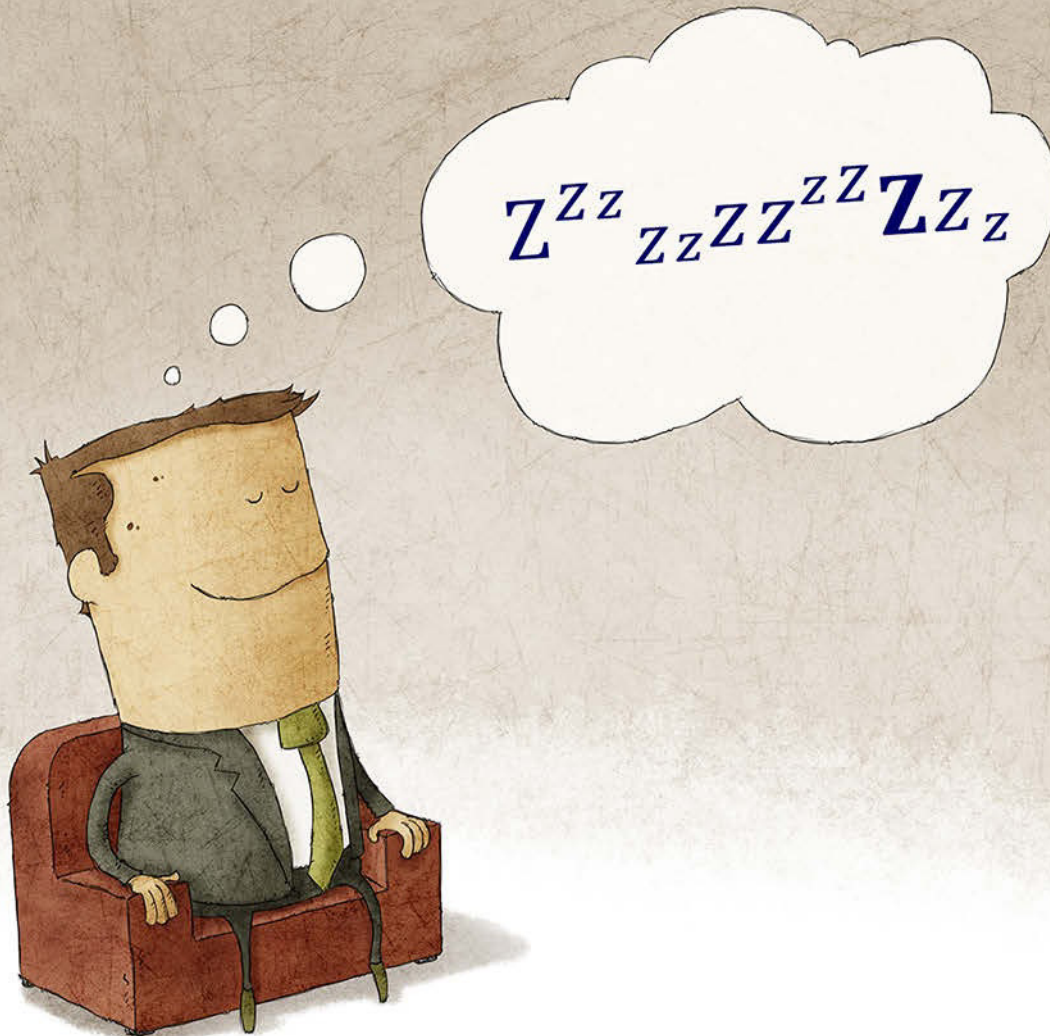
"We've heard many stories from people who rely on sleeping pills or excessive amounts of caffeine, and we wanted to provide something that would help people stabilize their biological rhythms in a more natural way," said Ardor, the founder and CEO of Luple.

Each device is compact, portable and can be used simply by placing it on its magnetic lid and angling the light at a tilt. Olly takes two hours to fully charge with a USB-C cable, and a single charge can run for six hours.

(Source: PRWEB)



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