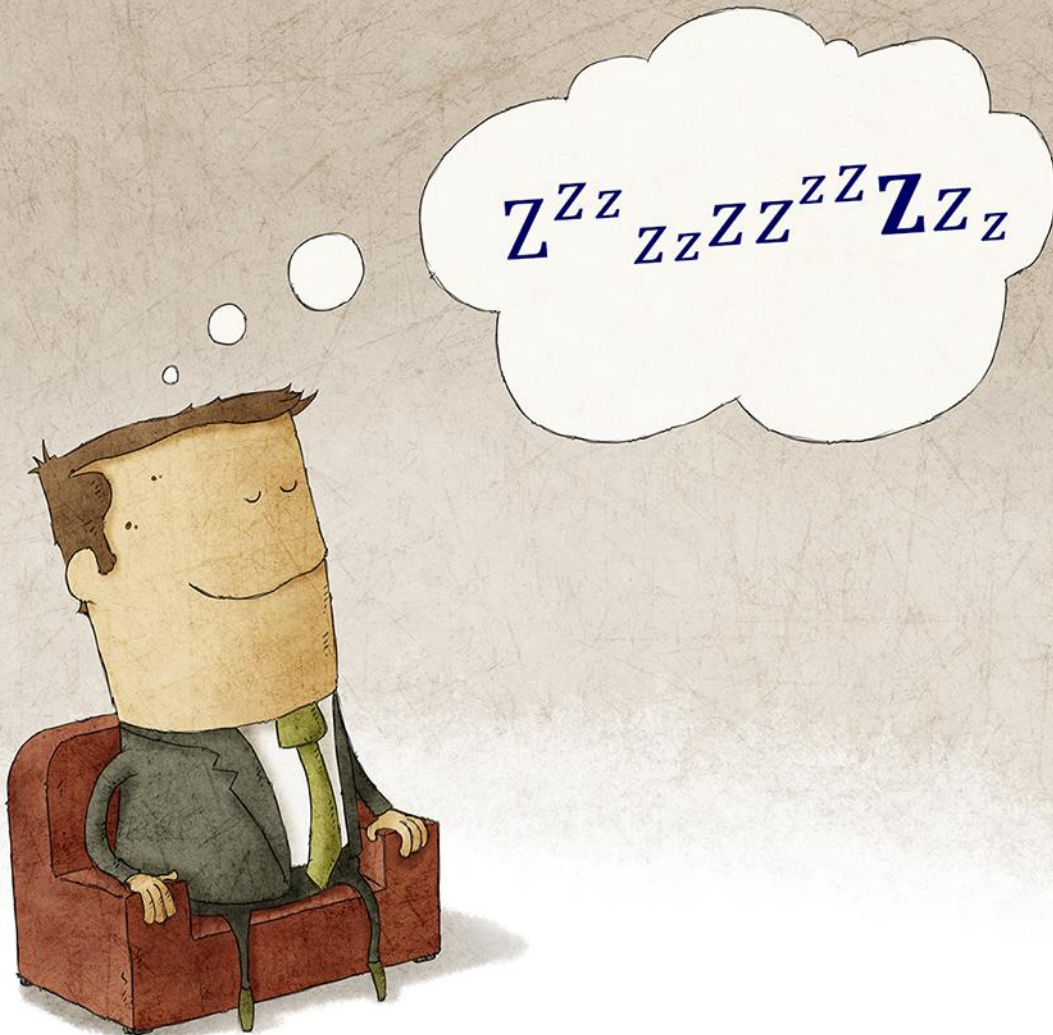


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- Power Distribution Network impedance

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– Barry Olney



AC/DC is not Just a Rock Band

Beyond Design

by Barry Olney, IN-CIRCUIT DESIGN PTY LTD / AUSTRALIA

Positioned at our usual table, directly in front of the stage at the local pub in Melbourne, Australia one Friday night in 1972, the boys and I laughed as a school boy, guitarist Angus Young, set up equipment and tuned a guitar. We assumed he was just one of the roadies, and were gobsmacked when the band unexpectedly fired up. High-voltage is not the word—more high-wattage, deafening—you could feel the sound as your ears distorted. The slick, gritty, blues-based lead riffs of the budding guitarist were insane. Little did we know that AC/DC's raucous image, with wild solo riffs, would make them one of the world's top heavy-rock bands. We willingly endured this every Friday night for weeks on end. Fortunately, the venue

was also a target-rich environment of eligible young ladies. In this month's column, I will discuss AC coupling (or is it DC blocking?) of high-speed serial links as my taste in music has matured over the years.

SERDES (serializer/deserializer) serial links are used to provide high-speed, high-bandwidth data transmission over differential signals and minimize the number of I/O pins and interconnects. And although it saves the PCB designer routing numerous parallel traces, implementing high-speed serial links can be challenging. Any small discontinuities in the physical geometries, along the transmission path, can significantly degrade the signal. This degradation includes loss of amplitude, reduction of



Figure 1: AC/DC fires up at an early gig (source: Kat Benzova).

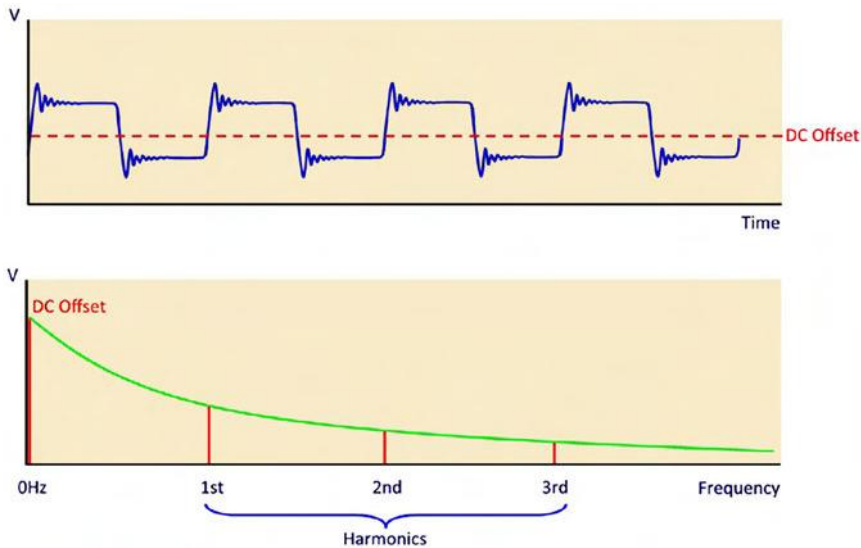


Figure 2: AC and DC components of a signal transferred to the frequency domain.

rise time, and increased jitter. As a result, one must be able to identify these discontinuities, in the high-speed channel, and mitigate their impact to improve the performance of the signal transmission.

A capacitor is typically placed in series with both differential signal traces to remove common mode voltage differences between ICs or different technologies. An “AC coupling capacitor” or “DC blocking capacitor” basically refers to the same thing. Any capacitor placed in series with the signal path tends to pass the high-frequency, AC portions of the signal, while simultaneously blocking the low-frequency DC portions. Since these capacitors couple transmitter to receiver, I prefer to use the term “AC coupling.”

In Figure 2 (top), the signal fluctuates about the DC offset. After performing a Fourier transform on a signal that consists of both AC and DC components, the DC component will be at 0Hz and the AC signal will be at its associated harmonic frequencies (bottom).

AC coupling is useful because the DC component of a signal acts as a voltage offset, and removing it can increase the resolution of the signal and allow different technologies to communicate without level shifters. Level shifter ICs can otherwise provide an interface between components that operate at different voltages. However, level shifters introduce delay varia-

tion (skew), increase power consumption, and are not suitable for low supply core voltages. AC coupling is needed to maintain the correct DC bias for receivers. If the transmitter has 0V DC bias and is of the same technology, then AC coupling does not have to implement.

The most important parameter, of the AC coupling capacitor, is the relative geometry with respect to the substrate. The capacitors are placed in series with high-speed traces and as such, the capacitor body becomes a section of transmission line. The equivalent series

inductance (ESL) of a capacitor, critical for bypass and decoupling applications, becomes negligible for AC coupling applications because the transmission line has inherent inductance anyway. Instead, the thickness of the stackup outer dielectric, trace width, land size, solder thickness and cover-layer thickness of the capacitor all interact together in the area of the capacitor.

In a well-matched interconnect, it does not matter where an AC coupling capacitor is placed. What does matter is how well the capacitor transition is designed, how low the reflectivity is, and whether it is placed near other channel discontinuities. Far away from other discontinuities is best.

AC coupling removes the common mode level and allows the receiver to set its own bias point. This is especially useful for rack-to-rack systems where the common mode cannot be well controlled. It also has the advantages of allowing:

- VTT referenced and GND referenced systems to work together
- A single SERDES channel to cover multiple standards
- Newer (restricted supply) devices to work with legacy devices
- The ability to hot-swap and protection from external shorts

However, AC coupling capacitors are common sources of impedance discontinuities in high-speed serial channels. Typically, narrow trace width and close trace spacing are used to construct the 100Ω differential transmission line pair. However, as these narrow trace pairs are routed into the surface mount lands of a capacitor, the sudden widening of the copper, as they join with the capacitor lands, causes an abrupt impedance discontinuity. The effect of this discontinuity appears as excess capacitance because the surface mount lands, of the capacitors, act as a parallel plate with the reference plane beneath.

To eliminate the excess parasitic capacitance, associated with surface mount lands, a portion of the reference plane, that is directly beneath the component, should be removed. This allows the signal that traverses through the capacitor

to reference a lower plane (further away) and reduces the parasitic capacitance, thereby minimizing the impedance mismatch. This principle should also be applied to surface mount connectors if present in the path (Figure 3).

On the left there are two capacitors which are referenced to the plane on layer 2. Whereas, the picture on the right shows the optimized structure with the plane cut outs included. The lands then reference to the layer 3 plane increasing the impedance. The board stackup and trace geometries (Figure 4) are designed to provide a 100Ω differential signal. All traces and plane layers are 1 oz. copper. The width of the surface mount lands is set to 20mils to match the width of the 0402 type capacitors. And, the length of the cut out is equal to the end-to-end distance of the two surface mount lands. The iCD Stackup Planner can be used

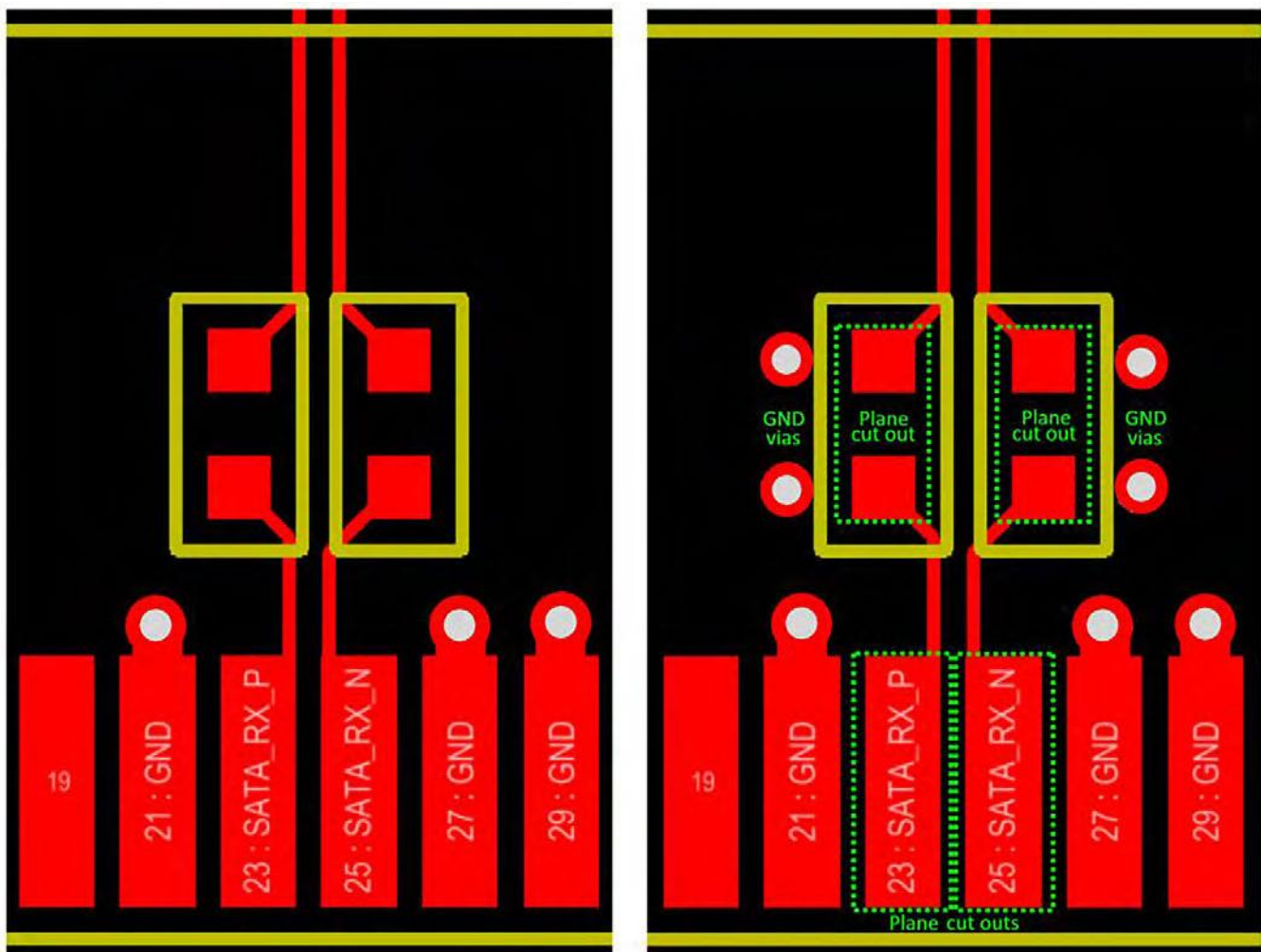


Figure 3: AC coupling capacitors (left) with plane cut-outs and GND vias (right).

Stackup Planner	PDN Planner	CPW Planner												
2 Layer	4 Layer	6 Layer	8 Layer	10 Layer	12 Layer	14 Layer	16 Layer	18 Layer	12 Layer acc					
UNITS: mil										2/5/2018		Total Board Thickness: 61.4 mil		
Differential Pairs >										100 ohm Differential				
Layer No.	Via	Description	Layer Name	Material Type	Dielectric Constant	Dielectric Thickness	Copper Thickness	Trace Clearance	Trace Width	Current (Amps)	Characteristic Impedance (Zo)	Edge Coupled Differential (Zdiff)	Broadside Coupled Differential (Zdbs)	
1	8	Signal	Top	Conductive			1.4	5	20	1	47.9	72.19		
		Prepreg		Dielectric	4.3	10								
2		Plane	GND	Conductive			1.4							
		Core		Dielectric	4.3	8								
3		Plane	GND	Conductive			1.4							

Stackup Planner	PDN Planner	CPW Planner												
2 Layer	4 Layer	6 Layer	8 Layer	10 Layer	12 Layer	14 Layer	16 Layer	18 Layer	12 Layer acc					
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1	8	Signal	Top	Conductive			1.4	5	20	1	70.07	100.34		
		Prepreg		Dielectric	4.3	10								
2		Signal	GND	Conductive										
		Core		Dielectric	4.3	8								
3		Plane	GND	Conductive			1.4							

Figure 4: 100Ω impedance when the plane beneath the capacitor is removed (source: iCD Stackup Planner).

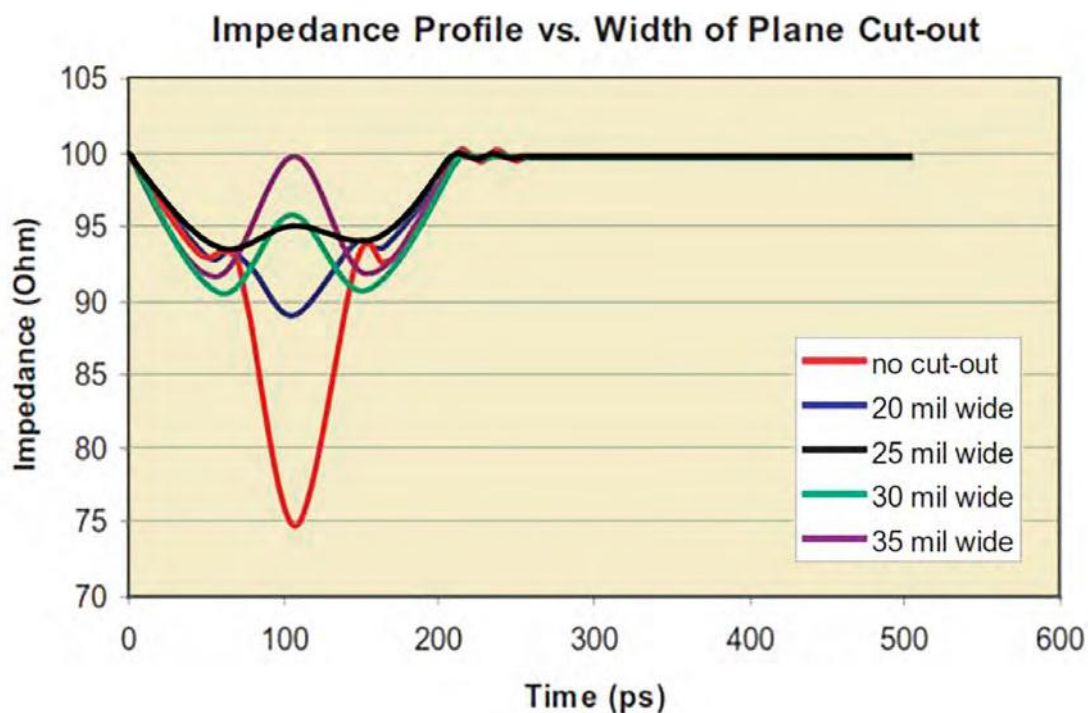


Figure 5: TDR simulation of impedance profile vs plane cut out width (source: Altera).

to estimate the impedance, to the lower plane on layer 3, by swapping the layer 2 plane for a signal layer as depicted. This increases the impedance from 72 to 100Ω.

The four ground vias near the AC coupling capacitors and the two on the connector lands, in Figure 3, are essential to provide a direct current return path to the lower GND plane

and back. Vias correctly placed will serve to minimize crosstalk and contain the common modes that propagate due to signal skew. Common mode conversion near the receiver can have some disastrous multi-aggressor crosstalk peaking implications.

Figure 5 shows a TDR impedance plot from an Ansoft HFSS simulation. The red line is the

impedance profile of the high-speed differential traces without the plane cut out under the surface mount lands of the AC coupling capacitors. The other lines are the impedance profiles with the cut out set to different widths.

The simulation results show that the width of the plane cut out plays an important role in minimizing the impedance mismatch. The impedance without the plane cut out is below 75Ω at the capacitor lands. However, this needs to be increased to 100Ω to avoid reflections. The minimum impedance mismatch and therefore the optimum structure is achieved when the width of the cut out is 25mils. For most applications, a capacitance value of 100nF with a 0402 package, for the AC coupling capacitor, is adequate.

This is a basic guideline to follow if you do not have access to a simulation tool. If the lower plane is a power plane or if there is no lower plane, a ground fill can be poured in the region underneath the capacitors and stitched with four GND vias close to each capacitor land.

Systems fail for all sorts of reasons, and some of the issues relate to the interaction between reflections across multiple components. Optimization is free, and margin-engineering is a non-recurring expense, and as such is free with regards to manufacturing costs. Once done, the margin is always there and costs nothing to implement.

Key Points

- Discontinuities in the physical geometries, along the transmission path, degrade the signal by loss of amplitude, reduction of rise time, and increased jitter.
- A capacitor is typically placed in series with both differential signal traces to remove common mode voltage differences.
- AC coupling is useful because the DC component of a signal acts as a voltage offset, and removing it can increase the resolution of the signal and allows different technologies to communicate.
- The most important parameter of the AC coupling capacitor is the relative geometry with respect to its environment.

- It does not matter where an AC coupling capacitor is placed along the transmission path.
- The capacitor transition is critical: how low the reflectivity is, and whether it is placed near other channel discontinuities.
- AC coupling removes the common mode level and allows the receiver to set its own bias point.
- To eliminate the excess parasitic capacitance, associated with surface mount lands, a portion of the reference plane, that is directly beneath the component, can be removed.
- Ground vias placed near the AC coupling capacitors are essential to provide a direct current return path to the lower GND plane and back.
- The minimum impedance mismatch and therefore the optimum structure is achieved when the width of the cut-out beneath the capacitor is 25 mils.
- For most applications, a capacitance value of 100nF with an 0402 package for the AC coupling capacitor is adequate.

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3. AC and DC Coupling: What's the Difference? Siemens.
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Barry Olney is managing director of In-Circuit Design Pty Ltd (iCD), Australia, a PCB design service bureau that specializes in board-level simulation. The company developed the iCD Design Integrity software incorporating the iCD Stackup, PDN and CPW Planner. The software can be downloaded from www.icd.com.au. To contact Olney, or read past columns, [click here](#).