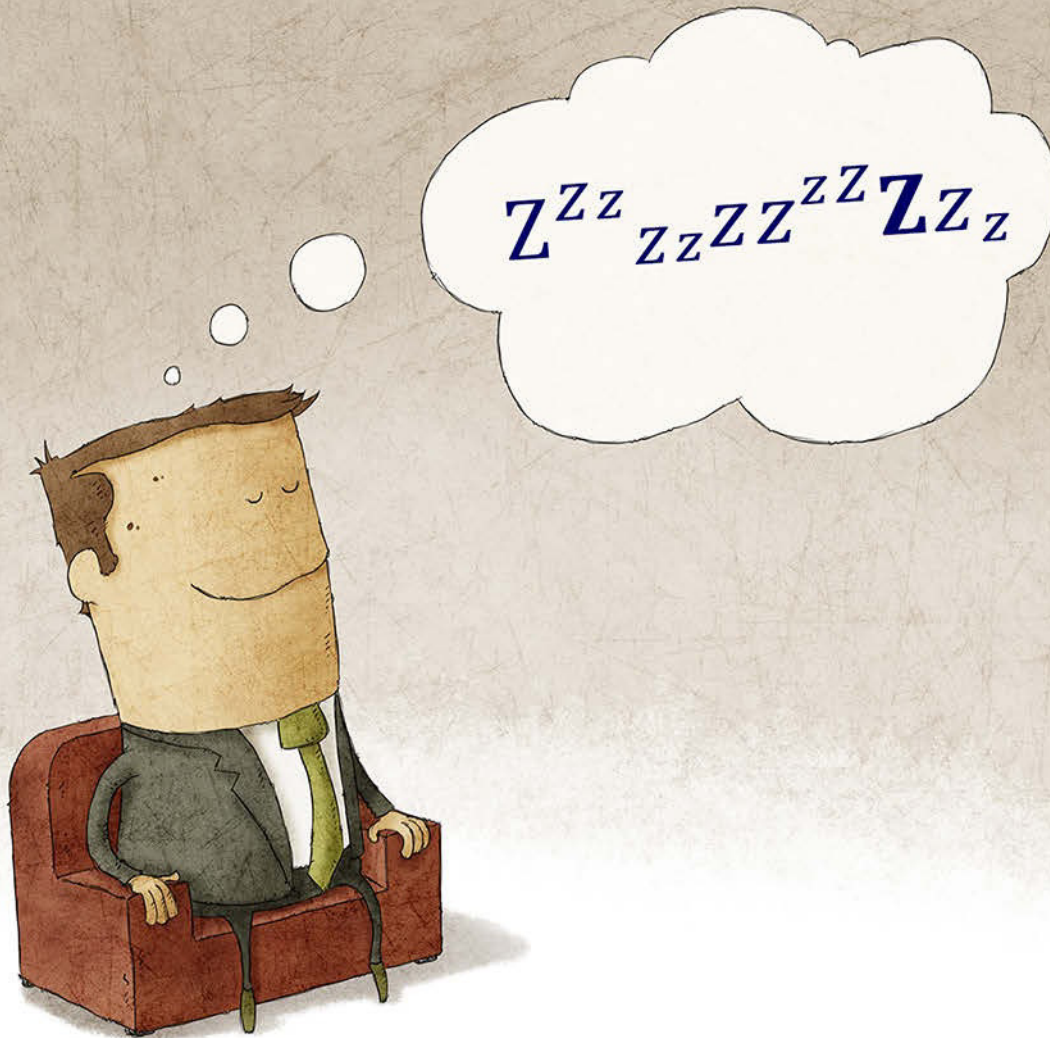


We **DREAM** Impedance!



Did you know that two seemingly unrelated concepts are the foundation of a product's performance and reliability?

- Transmission line impedance and
- Power Distribution Network impedance

DISCOVER MORE

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"iCD Design Integrity software features a myriad of functionality specifically developed for PCB designers."

– Barry Olney



Stackup Planning: Three Decades of Innovation

Beyond Design

Feature Column by Barry Olney, IN-CIRCUIT DESIGN PTY LTD / AUSTRALIA

The multilayer PCB is the most critical component of an electronics assembly. If it fails, your system fails! The PCB is so fundamental that we often forget that it is a component, and like all components, must be chosen based on specifications to achieve the best possible performance of the product.

Stackup planning involves careful selection of materials and transmission line parameters to avoid impedance discontinuities, signal coupling, unintentional return paths, high AC impedance and excessive electromagnetic emissions. Materials used for the fabrication of multilayer PCBs absorb high frequencies and reduce edge rates thus putting the materials selection process under tighter scrutiny. Ensuring that your board's stackup and impedances are correctly configured is a good basis for stable product performance.

In the late 1980s, my colleagues and I were designing relatively high-speed broadband

communications products (Figure 1). We knew that the impedance of the digital transmission lines had to be between 50–60 ohms but had no way of determining the exact value. Then, in April 1990, the IPC-D-317 standard was released. This was the first guideline for Electronic Packaging Utilizing High-Speed Techniques that incorporated transmission line equations. Problem solved?

However, punching the numbers of the lengthy equations into my scientific calculator seemed to always result in different values. As frustrating as this was, I tolerated it for years until finally in 1995 I had the idea to simplify the process by creating an online multilayer impedance calculator that everyone could use. This tool was based on the IPC-D-317 standard (now IPC-2251) closed-loop equations which are, in reality, just approximations—but it was the “best guess” for its time. Field solvers first appeared about five years later but were too expensive for the average punter.

Free online tools are great but to realize some return, in 2010 I imported the equations to a Windows application, coined the term “stackup planner” and started to build on its functionality. Later, a 2D Boundary Element Method (BEM) Field Solver was integrated into the iCD Stackup Planner to achieve industry-leading accuracy. iCD then continued to develop applications with high-speed design features specifically for PCB designers. These included the iCD PDN

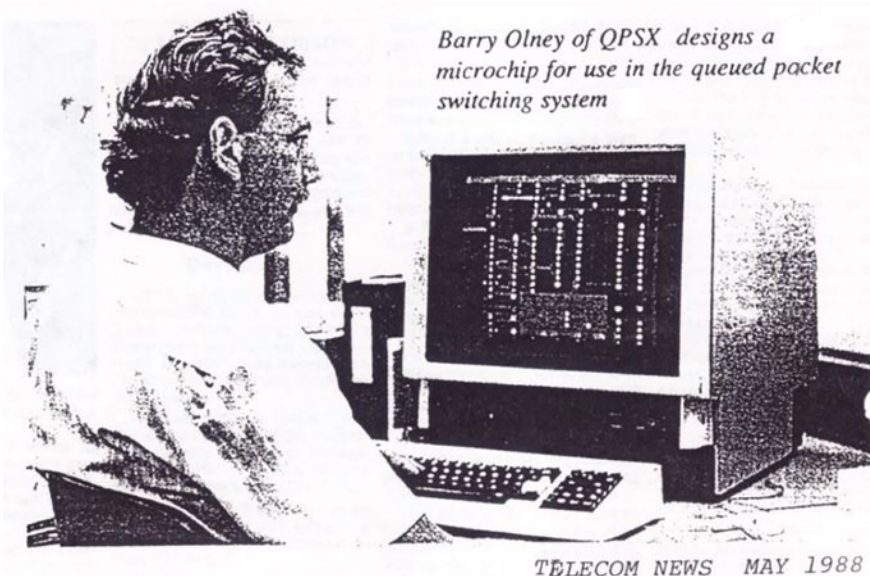


Figure 1: Designing a multilayer PCB using Daisy, Board Master, Unix software.

Planner, iCD Coplanar Waveguide Planner and the more recent iCD Materials Planner software.

Over the years, I have also written many stackup planning and material selection application notes and columns. Rather than repeat all the valuable points, made in these articles, I will list them below:

1. Arguably the most downloaded (and most plagiarized) is **Multilayer PCB Stackups**. You can find this article in numerous sites on the internet but sadly not attributed to me. It covers stackup planning basics and looks at the most common multilayer configurations (4-16 layers) and their associated pros and cons.
2. **The Perfect Stackup**: This application note discusses how to plan a multilayer PCB stackup to obtain the ideal stackup for high-speed design. Stackup Planning Parts 5 and 6 elaborate on this.
3. **Stackup Planning and the Fabrication Process**: Before starting a PCB design, we need to plan the PCB stackup for optimized performance, ensure that the selected substrate materials are available and clearly document the stackup so that it can be fabricated to engineering specifications.
4. **Stackup Planning Part 1**: The PCB substrate must be selected based on specifications to achieve the best possible performance of the product.
5. **Stackup Planning 2**: Comprises definitions of basic stackups starting with four and six layers. Of course, this methodology can be used for higher layer count boards—36, 72 layers and beyond.
6. **Stackup Planning Part 3**: Looks at higher layer-count stackups. As the layer count increases, these rules become easier to implement but decisions regarding return current paths become more challenging.
7. **Stackup Planning Part 4**: Ten plus layers require very thin dielectrics to reduce the total board thickness. This naturally provides tight coupling between the adjacent signal and plane layers reducing crosstalk and electromagnetic emissions.

8. **Stackup Planning Part 5**: To achieve the next level in stackup design, one needs to not only consider the placement of signal and plane layers in the stackup, but to visualize the electromagnetic fields that propagate the signals through the substrate.
9. **Stackup Planning Part 6**: Impedance variables. Interconnect Impedance is a trade-off between the variables—trace width, trace (copper) thickness, dielectric thickness and dielectric constant. Then, if you also need to include differential impedance, the trace clearance comes into play. For minimum crosstalk, coupling also must be considered.
10. **Material Selection for Digital Design**: What types of materials are commonly used for digital design and how to select an adequate material to minimize costs.
11. **Material Selection for SERDES Design**: Many challenges face the designer working with new technologies. For SERDES—high-speed serial links—loss, in the transmission lines, is a major cause of signal integrity issues. Loss can be mitigated by the correct selection of materials.
12. **It's a Material World**: Precise material selection is crucial to the performance of the today's multi-gigabit designs.

Design techniques constantly change and the current best practice for high-speed stackup design is:

- I. Closely couple GND/PWR planes on layers 2 and 3 and the second and third layers from the bottom (Figure 2). This lowers the AC impedance of the PDN and provides low inductance power to the devices.

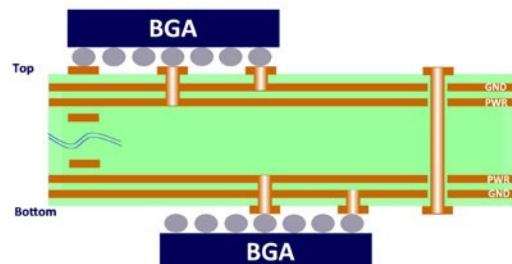


Figure 2: Plane pairs close to BGAs.

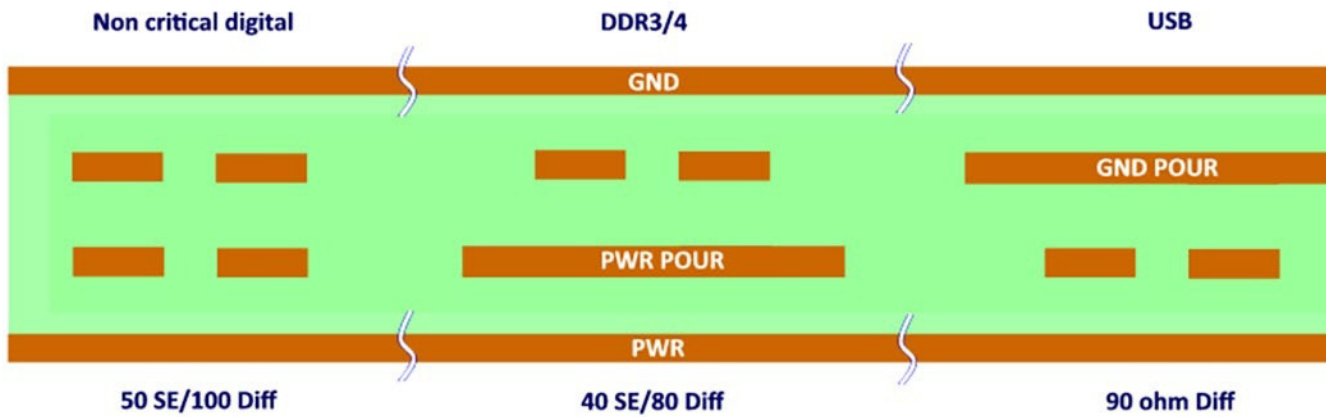


Figure 3: Three technologies accommodated on the same stripline layers.

II. Control electromagnetic fields by using dual stripline mixed signal/plane pour layers to isolate critical signals.

In Figure 3, there are three technologies on the same stripline layers. This is accomplished by using a combination of copper pours on one or the other signal layers. Trace width and spacing can also be modified to trim the impedance.

There are many advantages to this configuration including:

- This configuration isolates critical signals and accommodates all the necessary power supplies in complex designs
- DDR3/4 data or address busses can be routed on separate regions using the DDR supply and GND as reference planes
- Adjacent signal traces for the noncritical digital signals should be routed orthogonally to avoid crosstalk

III. Closely couple the signal layers to the reference planes to reduce crosstalk and radiation.

After reading all the above, you will now be extremely knowledgeable about stackup and material planning. But what is crucial for a good stackup design?

A. Field Solver Precision

As mentioned, closed loop equations are in reality just approximations. You can make do with approximations on low frequency, non-

critical designs but they just don't cut it in today's high-speed environment. Equations particularly come unstuck in dual asymmetric stripline configurations.

The most essential design tool for optimizing the stackup of a PCB is the 2D field solver (e.g. Figure 4). It is used to predict the characteristic impedance, edge-coupled and broadside coupled differential impedance for all topologies, including microstrip, stripline and dual stripline. In addition to the accuracy, the other advantage is its ability to include second-order effects such as trace thickness and the influence of air, solder mask, and multiple adjacent prepreg dielectrics. 3D field solvers are not more accurate than 2D field solvers in stackup design. When interconnects have a uniform cross-section, a 2D field solver can be more precise, faster and much easier to use.

To give you an idea, iCD now has a choice of over 700 series of rigid and flexible dielectric materials, from over 60 different manufacturers, in its dielectric materials library. When each material is used for the right target application, the resultant PCB will have the lowest possible cost while still satisfying the design and performance goals of the project. Choosing the best material for an application is often a daunting task. However, you can quickly sort through the vast array of choices, to make an informed decision, with the right tools.

Typically, when the impedance of a substrate is first calculated, virtual materials are used as the basis. In other words, we choose a

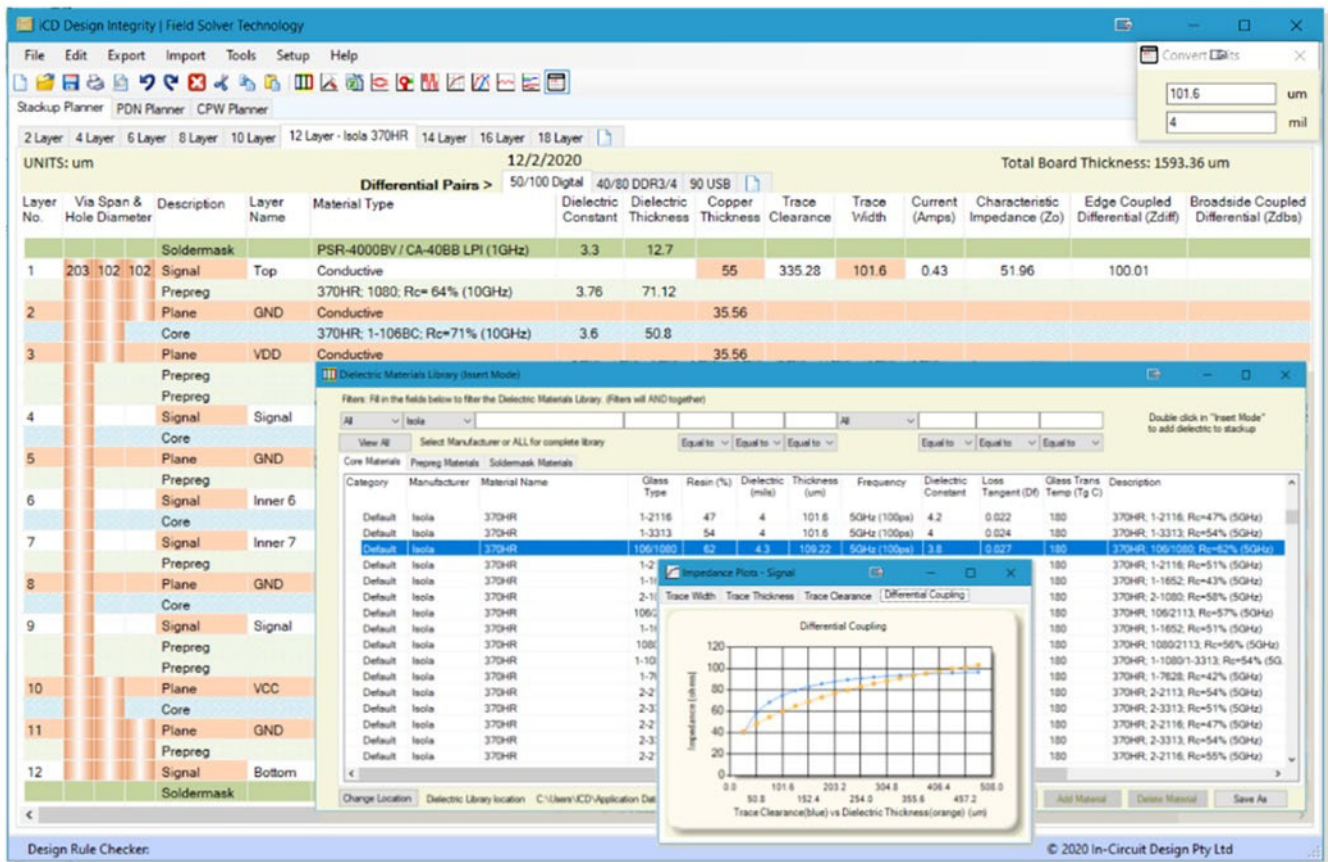


Figure 4: 2D Field Solver used to predict microstrip and stripline impedance (iCD Stackup Planner).

rough number to represent the dielectric constant, dielectric thickness, and the attributes of the trace thickness and width to establish a solution. However, these are not the attributes of the actual materials used by the fabricator to manufacture the board and are inherently inaccurate. There is no point in employing a field solver if your numbers are wrong.

Once the ballpark virtual material numbers are established, the material needs to be selected for the correct frequency of operation. Choosing the materials that are stocked will result in up to 5% better accuracy. Obviously, what you select is based on what is available at a reasonable price. Figure 5 is a graph of the low loss dielectrics stocked by a particular fabricator. One can clearly see which is the best material.

B. Incorporating Multiple Technologies

The iCD Stackup Planner is the first controlled impedance tool to enable field solver

computation of multiple differential pair definitions per layer. This allows you to incorporate differential 50/100 ohm Digital, 40/80 ohm DDR3/4, 90 ohm USB, etc., sharing the same layers (Figure 6). This is important as it is extremely rare to just have a 50-ohm single ended impedance. Usually, many different single-ended and differential impedances have to share layers throughout the substrate. And these variations have to be documented.

C. Seamless Integration to EDA software

For PCB designers, it is also important to be able to transfer the impedance variables and material properties to their EDA tools. Planning the PCB stackup in the early stages of the project reduces unnecessary iterations and optimizes the costs by increasing manufacturability and electrical performance. Far too many designers leave stackup design, which is critical to signal and power integrity, to the

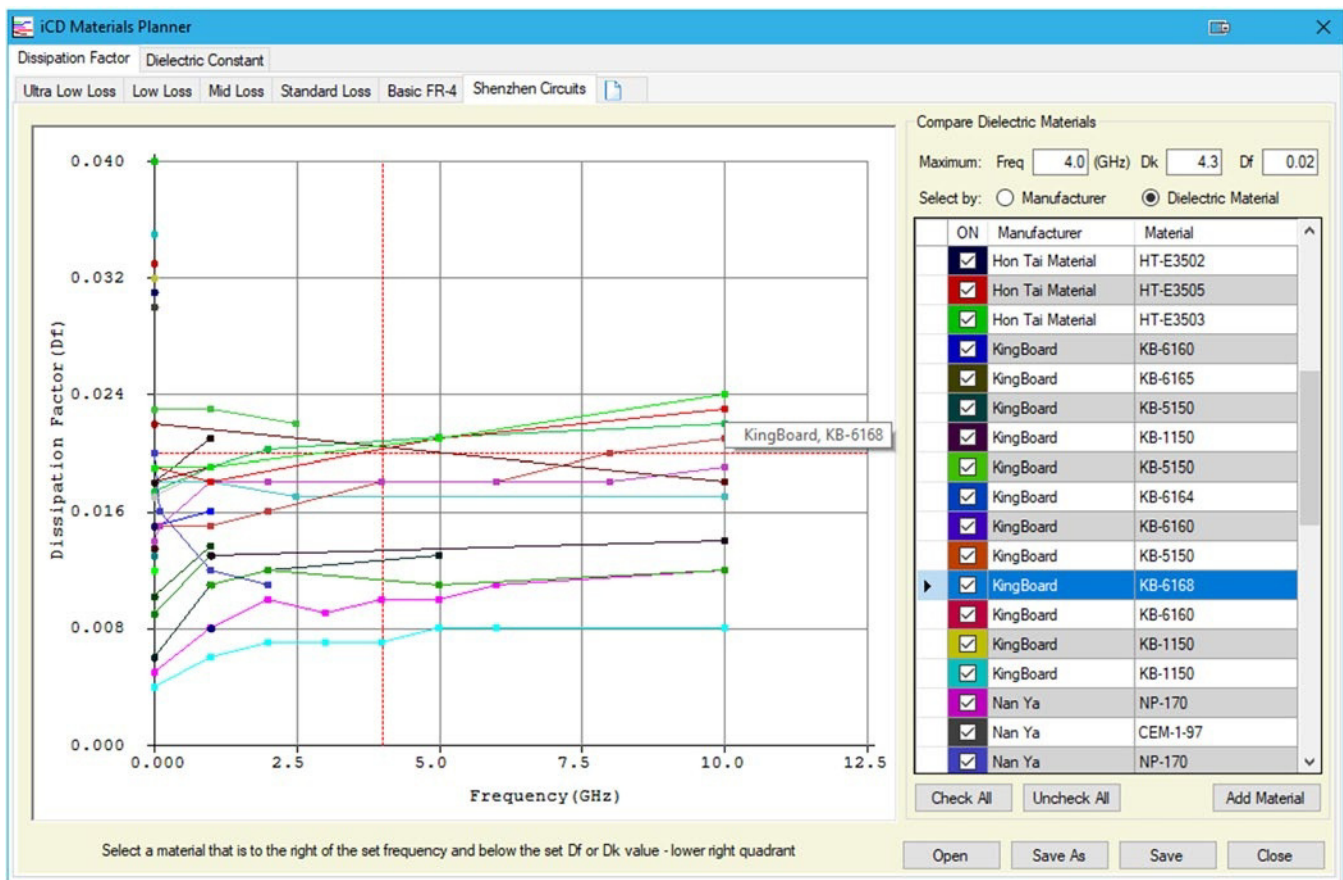


Figure 5: A fabricator's dielectric materials loss profile (iCD Materials Planner).

Differential Pairs >	50/100 Digital	40/80 DDR3	90 USB						
Material Type	Dielectric Constant	Dielectric Thickness	Copper Thickness	Trace Clearance	Trace Width	Current (Amps)	Characteristic Impedance (Zo)	Edge Coupled Differential (Zdiff)	
PSR-4000 HFX Satin / CA-40 HF LPI...	3.5	0.5							
			2.2	6	4	0.43	51.67	90.63	
			2.2	12	6	0.58	42.53	81.33	
			2.2	12	4	0.43	51.67	98.65	
370HR : 1080 ; Rc= 66% (1GHz)	3.97	2.9							
Conductive			1.4						

Figure 6: Multiple technologies on the same layer (iCD Stackup Planner).

PCB fabricators. The stackup should be created at the schematic capture stage and flow through the project to CAM deliverables. This avoids expensive design changes at the end of the project.

Stackup planning enables users to quickly explore alternatives in their substrate dimensions and material parameters to quickly assess the impact on performance. The right stackup strategy can reduce crosstalk and suppress EMI, ensuring that the signals will remain stable in the intended environment. **DESIGN007**

References:

1. *Beyond Design* by Barry Olney as referenced in the text.



Barry Olney is managing director of In-Circuit Design Pty Ltd (iCD), Australia. The company developed the iCD Design Integrity software incorporating the iCD Stackup, PDN, and CPW Planner is a PCB Design Service Bureau and specializes in board-level simulation. The software can be downloaded from www.icd.com.au. To read past columns or contact Olney, [click here](#).