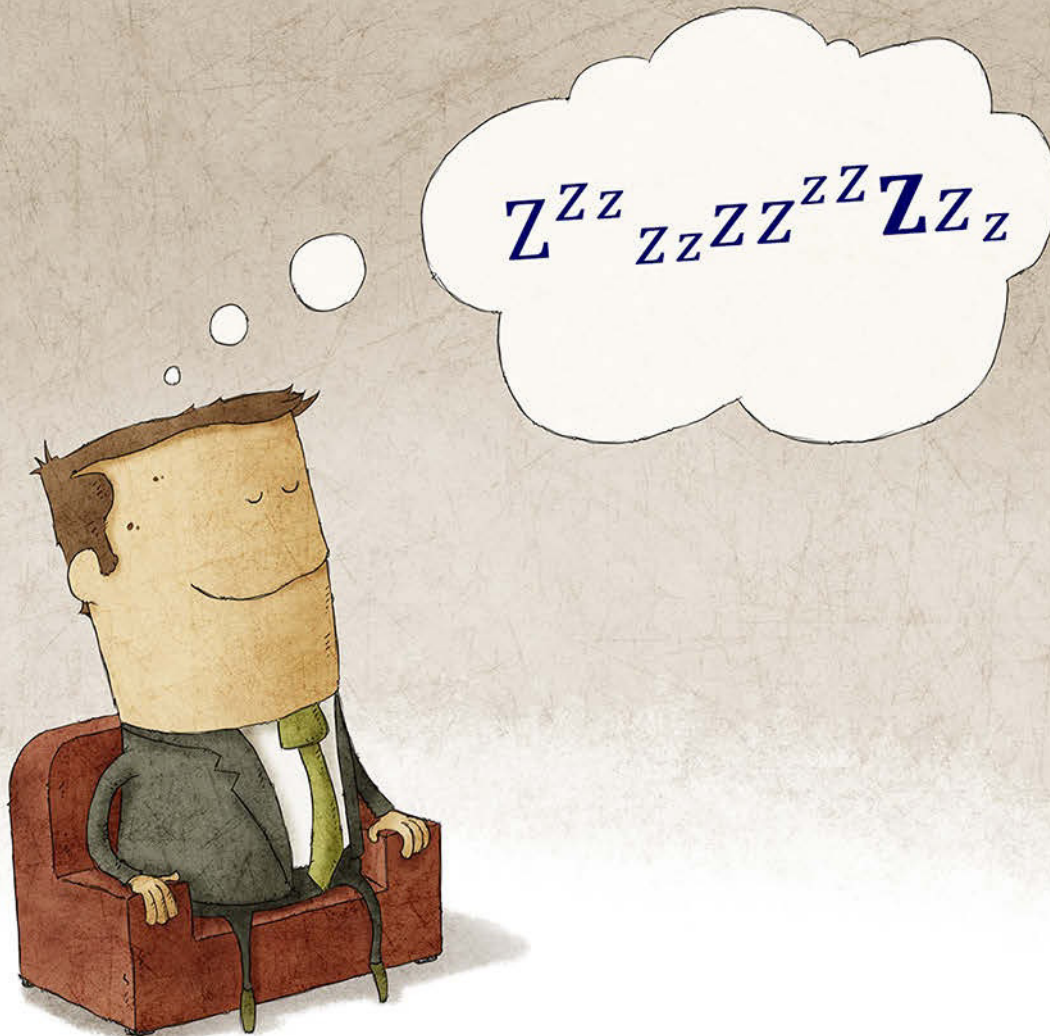


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10 Fundamental Rules of High-speed PCB Design, Part 5

Beyond Design

by Barry Olney, IN-CIRCUIT DESIGN PTY LTD / AUSTRALIA

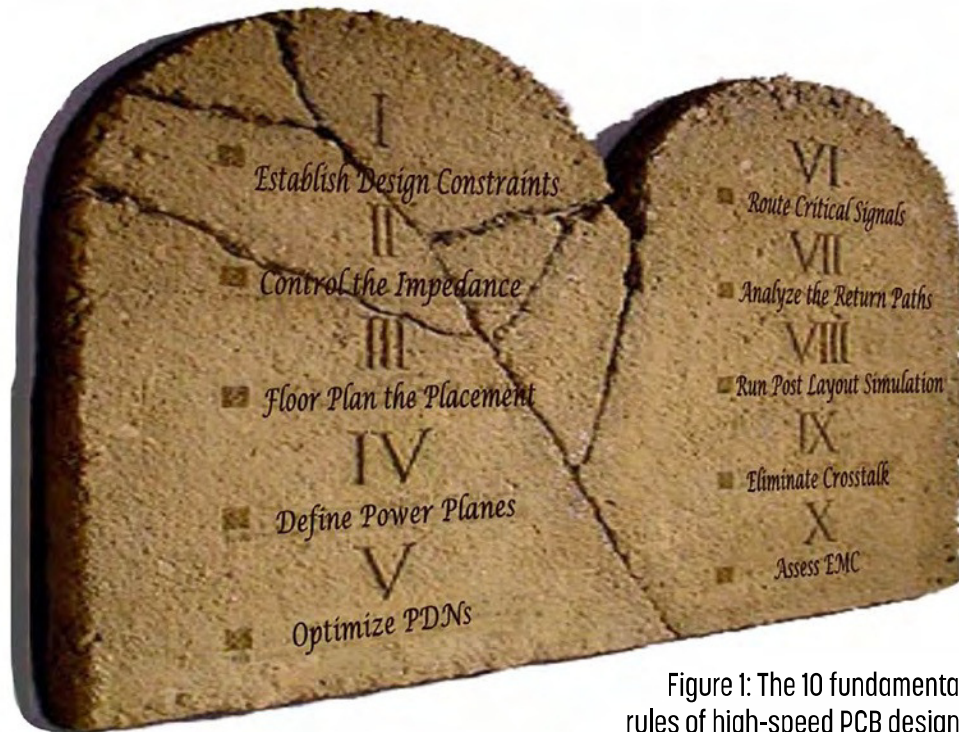


Figure 1: The 10 fundamental rules of high-speed PCB design.

The final part of the 10 fundamental rules of high-speed PCB design (Figure 1) focuses on board-level simulation encompassing signal integrity, crosstalk, and electromagnetic compliancy. Typically, a high-speed digital design takes three iterations to develop a working product. However, today, the product life cycle is very short, and therefore, time to market is of the essence. The cost per iteration should not only include engineering time but also consider the cost of delaying the products market launch. This missed opportunity could cost millions. Also, if an issue is not caught in the design phase and slips to through production and into the field, it could possibly damage a company's reputation.

Unfortunately, simulation is often engaged towards the end of the design cycle. Ideally, the

simulation should be done during the design process as part of standard practice. However, post-layout simulation is still necessary to validate the final signal and power integrity.

Board-level simulation cuts costs and a pre-layout simulation identifies issues in the conceptual stage so that they can easily be avoided. Post-layout simulation catches the issues during the design process, eliminating the potentially disastrous final stage changes.

VIII. Run the Post-layout Simulation

Simulate critical signals and match signal propagation and timing. Check for signal ringing and eye jitter.

The eye diagram (Figure 2) is a common indicator of the quality of a signal in high-speed digital transmission lines. In an ideal world, eye diagrams would look like rectangular boxes. In

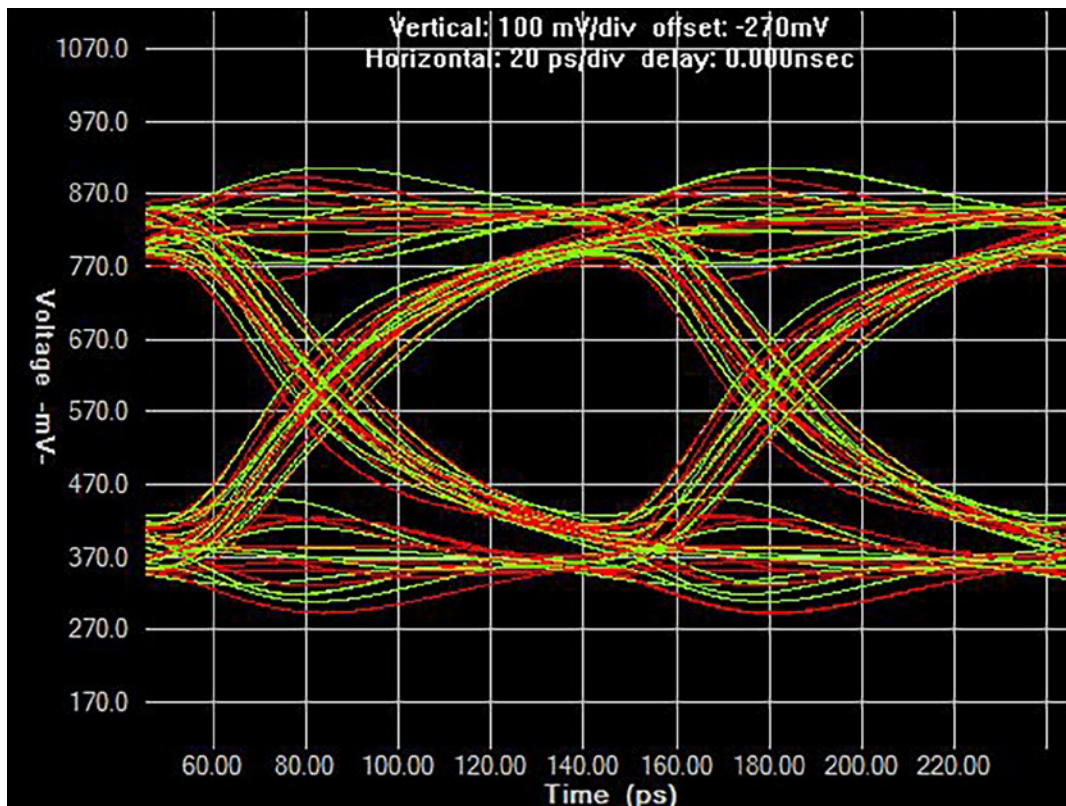


Figure 2: Eye diagram indicating signal quality (Figures 2-6 simulated in HyperLynx).

reality, data transmission is imperfect, so the transitions of the bit pattern do not perfectly align on top of each other, and an eye-shaped pattern results. An open-eye pattern with little jitter (horizontal disparity) and noise (vertical deviation) is the objective.

To attain this objective one needs to consider all the previous fundamental rules particularly:

- Control the impedance.
- Match the driver to the transmission line impedance.
- Tightly couple all signal traces to a contiguous reference plane and have a clearly defined minimum loop inductance return current path.
- Maintain constant impedance along the entire length of differential pairs.
- Synchronous data and address buses, plus associated clocks and strobes, should have matched propagation within their timing margin.

A preliminary batch mode simulation should initially be completed on the design. Default IC

characteristics, crosstalk of 150mV maximum and EMC to FCC or CISPR Class A and B, are set up in the simulator. The batch mode simulation automatically scans large numbers of nets on an entire PCB, flagging signal integrity, crosstalk, and EMC hot spots.

The post-layout simulation analysis can then be prepared using supplied specifications. This is an extensive interactive board level simulation which takes the analysis to the next level—simulating trouble spots identified by the batch analysis to further resolve the issues with greater accuracy. Keep in mind that any signal integrity concern will create issues downstream with ringing causing excessive crosstalk leading to electromagnetic radiation. Each issue should be dealt with one-by-one until they are all resolved.

Flight times of the critical signals should be examined thoroughly. One could compare the matched lengths of each signal, but the delay will vary depending on the meander pattern and the signal layer in the stackup. Also, the trace either side of a series terminator needs to be added to obtain the total delay. So instead,

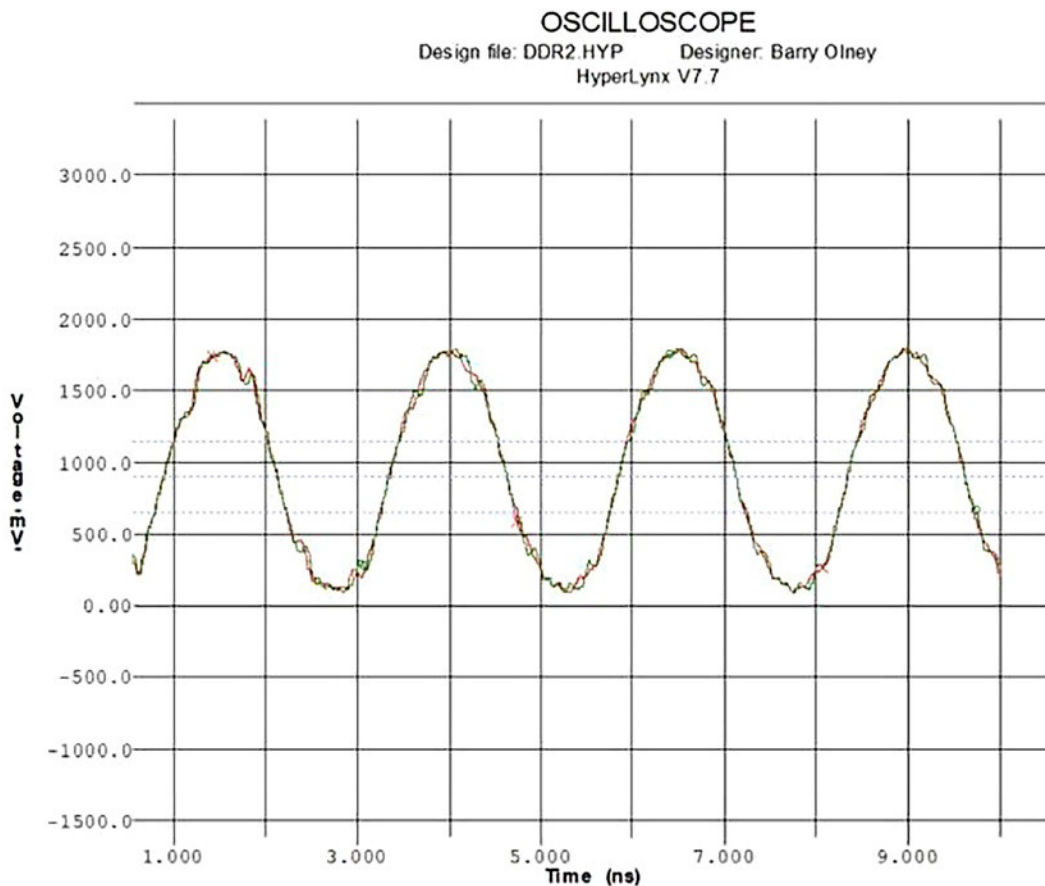


Figure 3: Flight times of data compared to strobe.

it is best to compare the skew between, for example in Figure 3, the MDQ0 (data) and MDQS0 (strobe) at the receiver to ensure the flight times are correct. In this case, there is 10pS difference, so this is well within the timing specification.

IX. Eliminate Crosstalk

Scan the board for possible crosstalk. Crosstalk can be coupled trace-to-trace on the same layer or broadside coupled by traces on adjacent layers.

Crosstalk is caused by the coupling of the electromagnetic fields. Electric fields cause signal voltages to capacitively couple into nearby traces. Capacitive coupling draws a surge of drive current which causes reflections on the transmission lines. Whereas, magnetic fields cause signal currents to be induced into nearby traces. Inductive coupling produces ground bounce and power supply noise. Crosstalk falls off rapidly with the square of the distance, and

the degree of impact is related to the aggressor signal voltage, available board real estate and thus the proximity of signal traces.

Crosstalk can be coupled trace-to-trace on the same layer (Figure 4) or can be broadside coupled by traces on adjacent layers (Figure 5). The coupling is three dimensional. Broadside coupling is difficult to spot as generally we look for trace clearances when evaluating crosstalk, but a simulator will pick this up. Traces routed in parallel and broadside cause greater amounts of crosstalk than those routed side-by-side due to the greater coupling area. Therefore, it is good practice to route adjacent signal layers in the stackup orthogonally to each other to minimize the coupling region. A better solution is to only have one signal layer between two planes to avoid broadside coupling altogether.

When interactive routing, one tends to group signals for aesthetic reasons—this is the artistic side of the PCB Designer showing through.

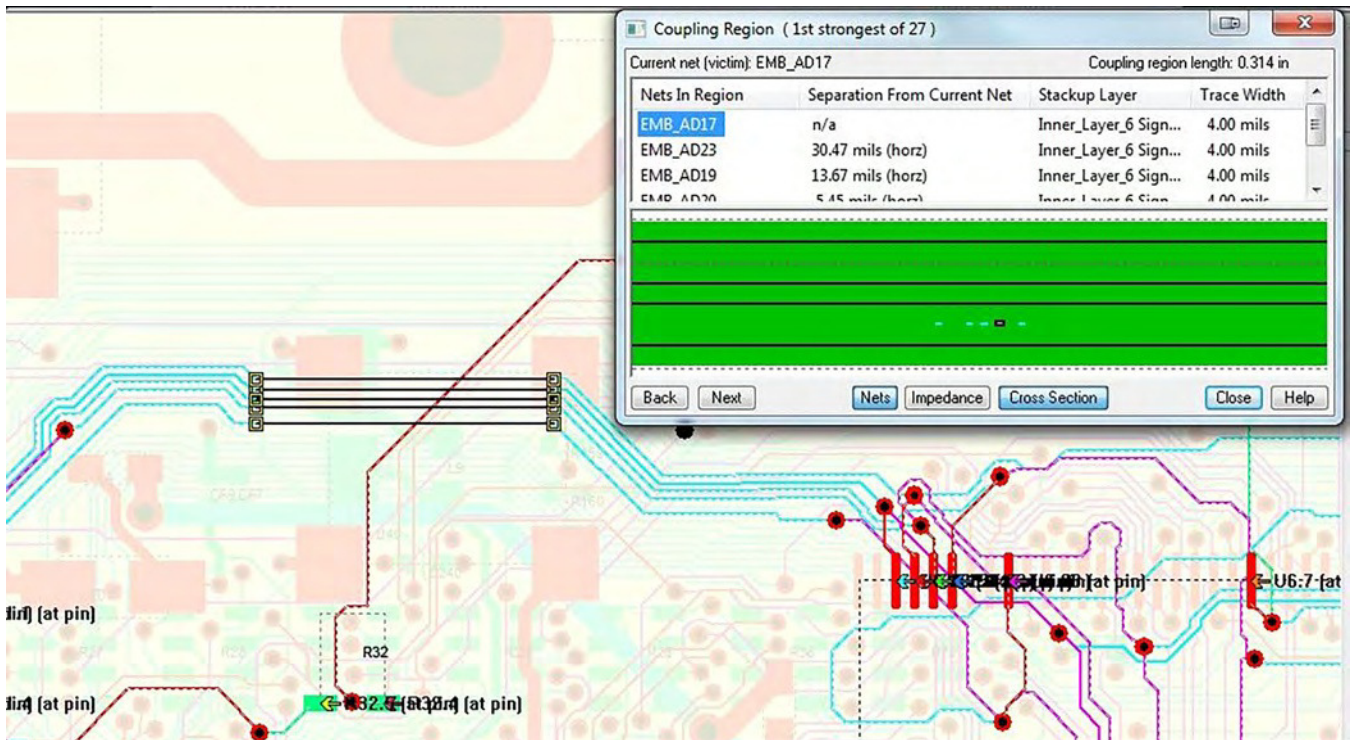


Figure 4: A walk through the coupling regions.

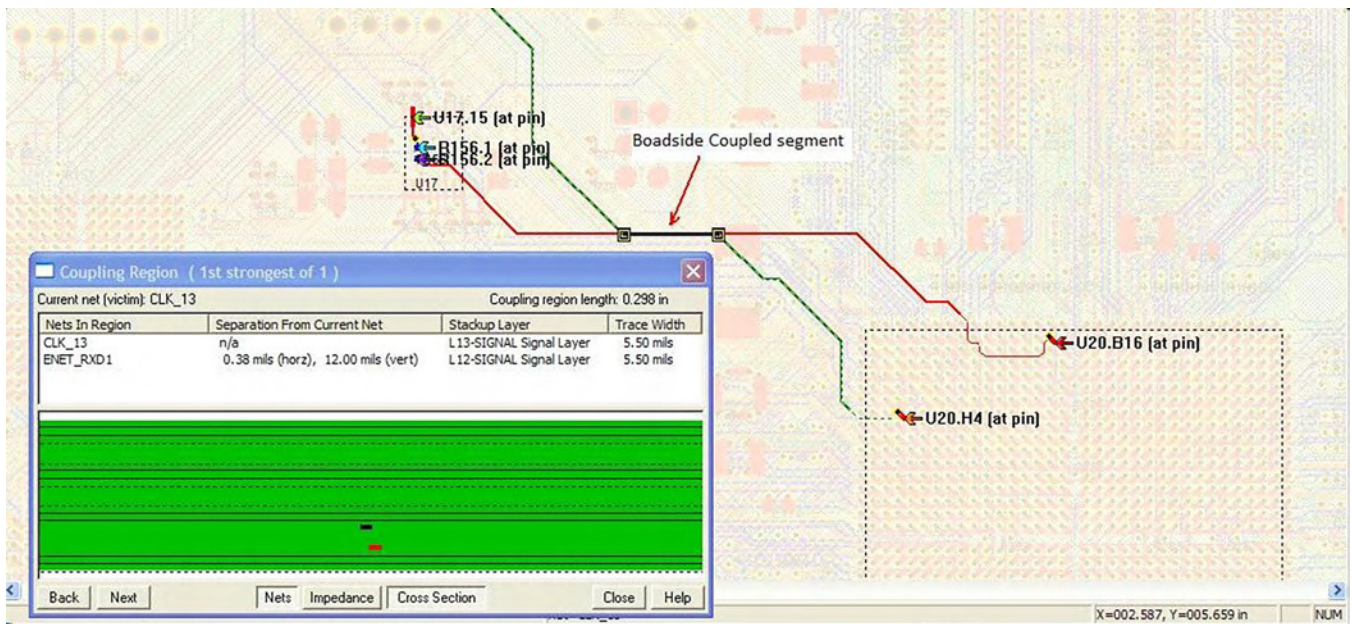


Figure 5: Broadside-coupled crosstalk.

But, although it looks nice and neat, it may not perform so well.

It is recommended that critical trace segments should be spaced by three times the trace thickness, where possible; alternatively, the trace to plane height can be reduced in the stackup if real estate is limited.

X. Assess Electromagnetic Compliancy (EMC)

Control EM radiation at the source. Ensure that differential mode signals do not convert to common mode and eliminate any possible antennae.

To be prudent, it is best to design the PCB layout with electromagnetic compatibility in mind rather than to be faced with excessive emissions at the prototype stage, or worse still, just before production. Unfortunately, too many of the problems are uncovered at the testing stage. Shielding and absorbing materials are then often used to reduce the emissions.

The preferred approach is to identify the problems at the board level and to rectify them there. Even then, if particular offending frequencies are identified, engineers are still faced with the nightmare of locating which net segments are the cause of these particular emissions.

Once excessive emissions are detected, the goal is to quench these emissions. Crude techniques involve the design of sealed enclosures, chokes and ferrites to restrain the launching of common-modes along cables and a variety of other methods that are too little and

too late. Alternatively, and more proactively, designers recognize that the problem should be addressed at the board level where the radiation emanates.

Since all products must comply with strict EMC regulations, all critical high-speed signals should be simulated to determine the amount of expected radiation. The EMC standards for FCC Class B limit the radiation to a 54-dB average with a peak of 74 dB (at a 3-m distance) above 1 GHz. However, harmonics can still cause unforeseeable problems (Figure 6). Generally, these issues are caused by routing traces on the outer (microstrip) layers where radiation is much higher than that of the inner (stripline) layers. Routing critical signals between the planes can reduce the EMI by more than 10 dB.

Electromagnetic radiation from differential pairs can occur as either differential or common mode. Differential mode is typically equal and opposite, and therefore, any radiating fields will

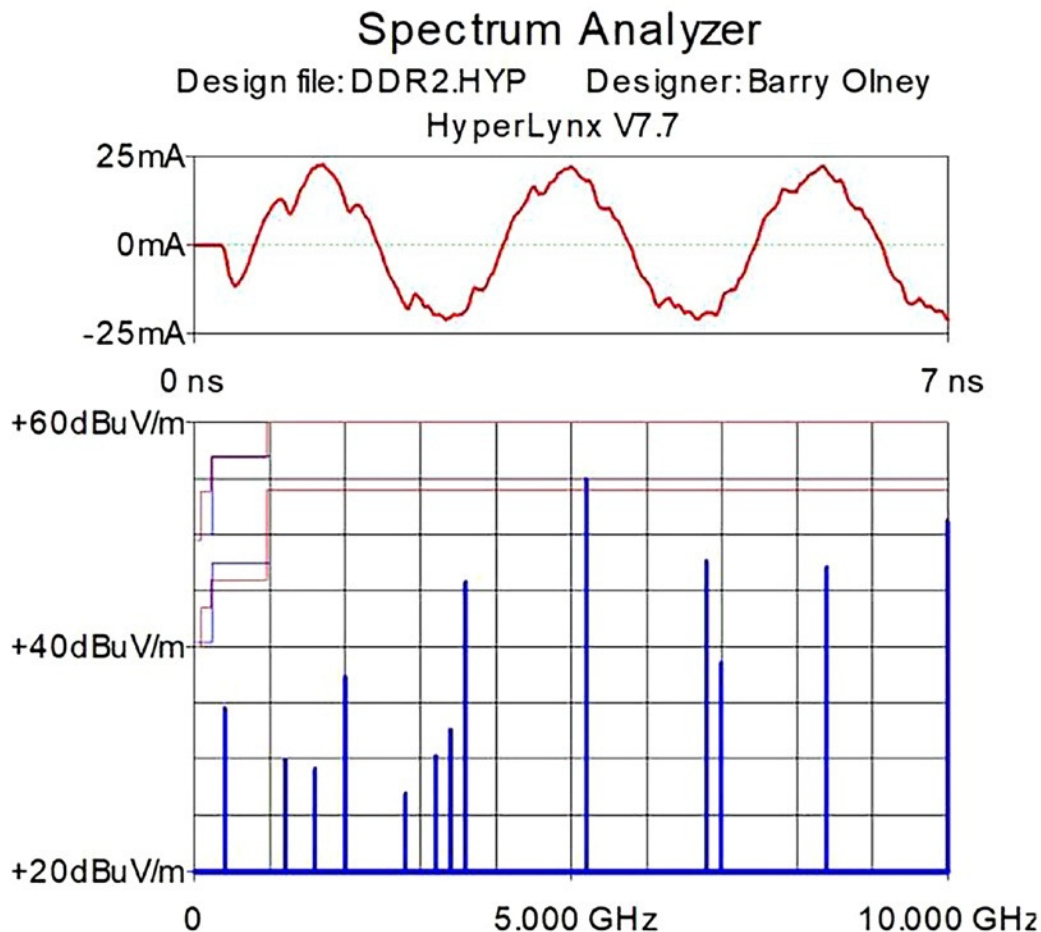


Figure 6: Electromagnetic radiation from MDQSO strobe.

cancel. Conversely, common-mode radiation from two coupled conductors is identical; it does not cancel, but reinforces. Unfortunately, differential-mode propagation can be converted to common mode by parasitic capacitance or any imbalance caused by signal skew, rise-fall time mismatch, or asymmetry in the channel.

Also, dangling via stubs distort signals passing through an interconnect and also decrease the usable bandwidth of the signal. This is due to the via stub acting as an antenna, which has a resonant frequency determined by the quarter wavelength of the structure. The conventional solution to this problem is to back-drill (or control depth drill) the vias to bore out the via stub barrel, so that the via stubs are reduced in length if not completely removed.

The Zeroth Rule

In [Part 1](#) of this series, I mentioned that there is always room for one more rule at the top, and this rule may be the foundation of earlier rules.

The most important rule is to scrutinize the design proactively as it unfolds, so you have the ultimate control over the outcome. Do not totally rely on the tools. High-speed PCB design is not just a process. As we all know, things can and do go horribly wrong at times. You cannot teach people to be good PCB designers. I have presented many training courses over the years, and unfortunately, individuals, although very capable, just don't have what it takes.

A successful high-speed PCB designer must:

- Communicate well with others within the team and the industry
- Appreciate the challenge and have good problem-solving skills
- Be creative and thorough, and pride yourself in the quality of your work
- Understand and implement IPC design standards and project-specific requirements
- Have a thorough knowledge of your EDA tools and PCB fabrication, assembly, and testing processes
- Understand transmission-line signal propagation, controlled impedance, and

recognize where signal currents flow and how coupling occurs at high frequencies

- Keep an eye on the ball during the entire design process, catching any small issues before they become a major problem

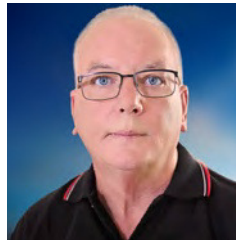
But what really makes an exceptional PCB designer? Ability must align with enthusiasm!

Key Points

- Simulation should be done during the design process as part of standard practice
- The eye diagram is a common indicator of the quality of a signal in high-speed digital transmission lines
- Any signal integrity concern will create issues downstream with ringing causing excessive crosstalk leading to electromagnetic radiation
- It is best to compare the skew between signals at the receiver to ensure the flight times are correct
- Crosstalk can be coupled trace-to-trace on the same layer or broadside coupled by traces on adjacent layers
- Traces routed in parallel and broadside cause greater amounts of crosstalk than those routed side-by-side due to the greater coupling area
- To reduce crosstalk, critical trace segments should be spaced by three times the trace thickness where possible; alternatively, the trace to plane height can be reduced in the stackup if real estate is limited
- It is best to design the PCB layout with electromagnetic compatibility in mind
- Proactive designers recognize that an EMC problem should be addressed at the board level where the radiation emanates
- Routing critical signals between the planes can reduce the EMI by more than 10 dB
- Differential-mode propagation can be converted to common mode by parasitic capacitance or any imbalance caused by signal skew, rise-fall time mismatch, or asymmetry in the channel
- Dangling via stubs distort signals passing through an interconnect and also decrease the usable bandwidth of the signal

Further Reading

- [Beyond Design: Crosstalk Margins](#) by Barry Olney, *Design007 Magazine*, July 2018.
- [Beyond Design: How to Handle the Dreaded Dangers, Part 2](#) by Barry Olney, *The PCB Design Magazine*, September 2016.
- [Beyond Design: Introduction to Board-level Simulation and the PCB Design Process](#) by Barry Olney, *The PCB Magazine*, March 2012.
- [Beyond Design: Board-level Simulation and the Design Process, Plan B—Post-layout Simulation](#) by Barry Olney, *The PCB Magazine*, February 2012.
- [Beyond Design: Controlling the Beast](#) by Barry Olney, *The PCB Magazine*, December 2011.
- [Beyond Design: Common Symptoms of Common-mode Radiation](#) by Barry Olney, *Design007 Magazine*, May 2018.
- “Board-level Simulation” by Barry Olney, *Electronics News (Australia)*, January 2013.
- “EMC Simulation Techniques for Printed Circuit Boards” by Dr. Al Wexler, Quantic EMC Inc. **DESIGN007**



Barry Olney is managing director of In-Circuit Design Pty Ltd (iCD), Australia, a PCB design service bureau that specializes in board-level simulation. The company developed the iCD Design Integrity software incorporating the iCD

Stackup, PDN, and CPW Planner. The software can be downloaded from www.icd.com.au. To read past columns or contact Olney, [click here](#).

Disposable Health Patch to Measure Vital Signs

At CES 2019 in Las Vegas, imec and TNO are presenting the latest version of their health patch. Developed in the framework of the Holst Centre in Eindhoven, the new health patch offers unprecedented comfort and a long battery life, previously unseen in this type of device. It can also be manufactured at a fraction of the cost of previous generations.

The patch uses a mix of skin friendly and biocompatible materials. A comfortable silicone adhesive is used to

provide long-term adhesion at high comfort. “Completely watertight, the new health patch is built for maximum user comfort and can be worn for up to seven days before needing to be replaced,” explains Prof. Jeroen van den Brand, program director of printed electronics, TNO.

For patients, a single, disposable patch that can be worn for several days is more convenient and can reduce hospital visits as it no longer needs to be returned after use. This is particularly important for chronically ill patients as it provides an affordable, single-use device that can be easily used to monitor their vital signs and physical activity at home. Easy to apply and comfortable to wear for long periods of time, it enables patients to perform their normal daily activities with minimal impact while providing valuable information to optimize their treatment and medication. The single-use concept can also reduce time spent in the hospital as it allows patients to be sent home earlier while still remotely monitoring their vital signs.

(Source: Holst Centre)

