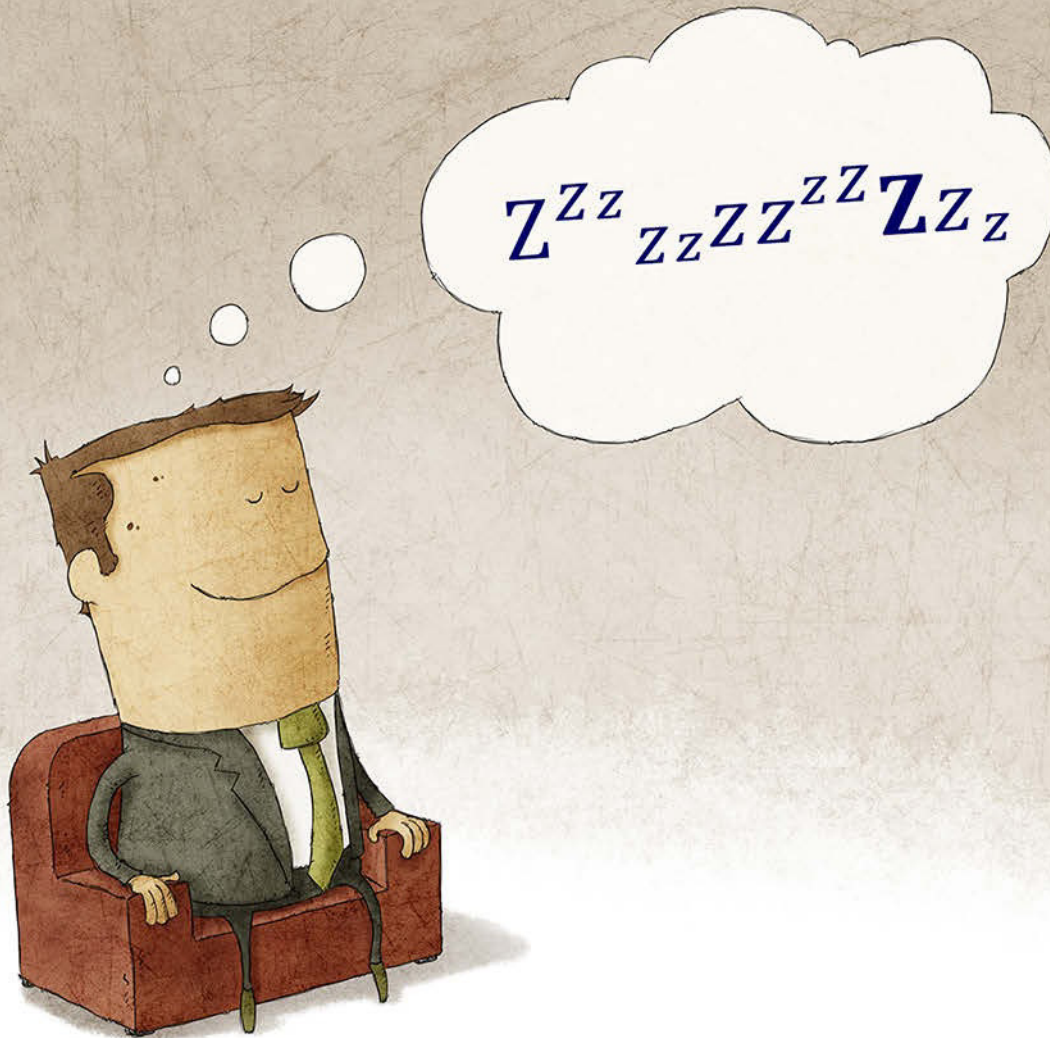


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10 Fundamental Rules of High-speed PCB Design, Part 4

Beyond Design

by Barry Olney, IN-CIRCUIT DESIGN PTY LTD / AUSTRALIA

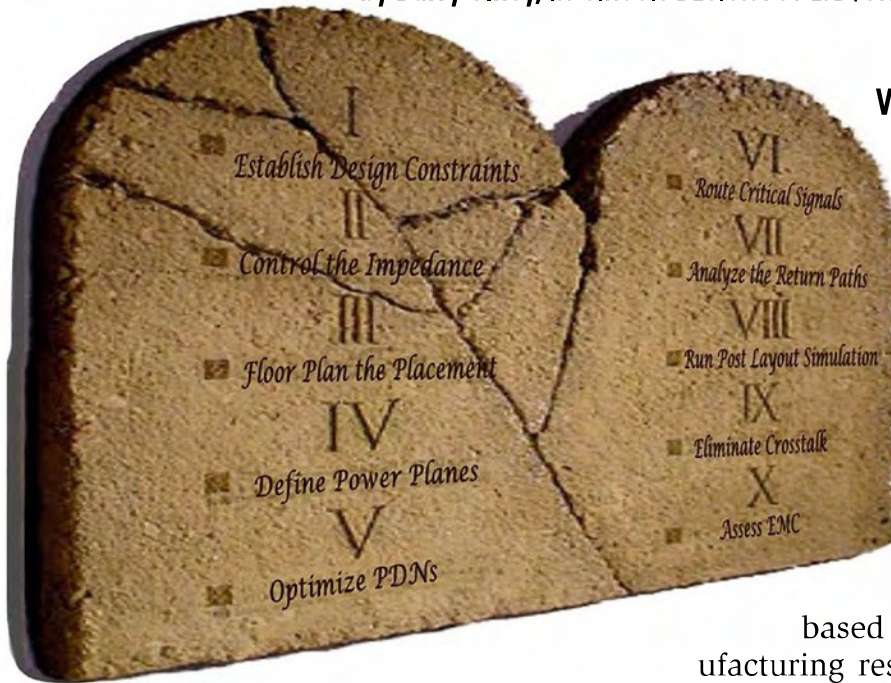


Figure 1: The 10 fundamental rules of high-speed PCB design.

Part 4 of the 10 fundamental rules of high-speed PCB design (Figure 1) deals with the routing of critical signals and return path discontinuities. Needless to say, matched delay and length, differential pairs, and other critical signals should be routed first with the precision they require before less important low-speed and static signals are completed. Maintaining this priority is imperative.

Note that the logic schematic diagram masks details crucial to the operation of unintentional signal pathways vital to the understanding of signal performance, crosstalk, and electromagnetic radiation emanating from the board. Therefore, it is just as important to understand the flow of the return current path of critical signals because these can influence the signal integrity and electromagnetic compliance (EMC).

VI. Route the Board Based on Critical Signals:

Adhere to the defined routing strategy. Clock signals should always have the longest delay of the group. Differential pairs should maintain constant impedance along the entire length.

As mentioned in [Part 1](#) of this series, before starting placement and routing, detailed interconnect routing constraints should be established. These constraints—

based on pre-layout simulation, manufacturing restrictions, and the IC manufacturer's recommendations and guidelines—will control the placement and routing processes. Online design rule checks (DRCs) will warn the designer when a constraint is violated.

When we draw a schematic by functionality, I think that we should also place and route by functionality. By doing this, you can add your own creativity and make decisions on the fly while still taking advantage of the automation. The most efficient approach is to cross-probe between the schematic and the PCB/routing editor (Figure 2). Also, having two extended monitors or a new 34-inch curved screen monitor—as I just purchased—makes this very easy to implement. I read that curved monitors make a straight line look bent and are not suitable for CAD applications. However, that is definitely not the case as the screen curvature follows the natural profile of the eye and the graphics appear crystal clear and undistorted over the entire screen.

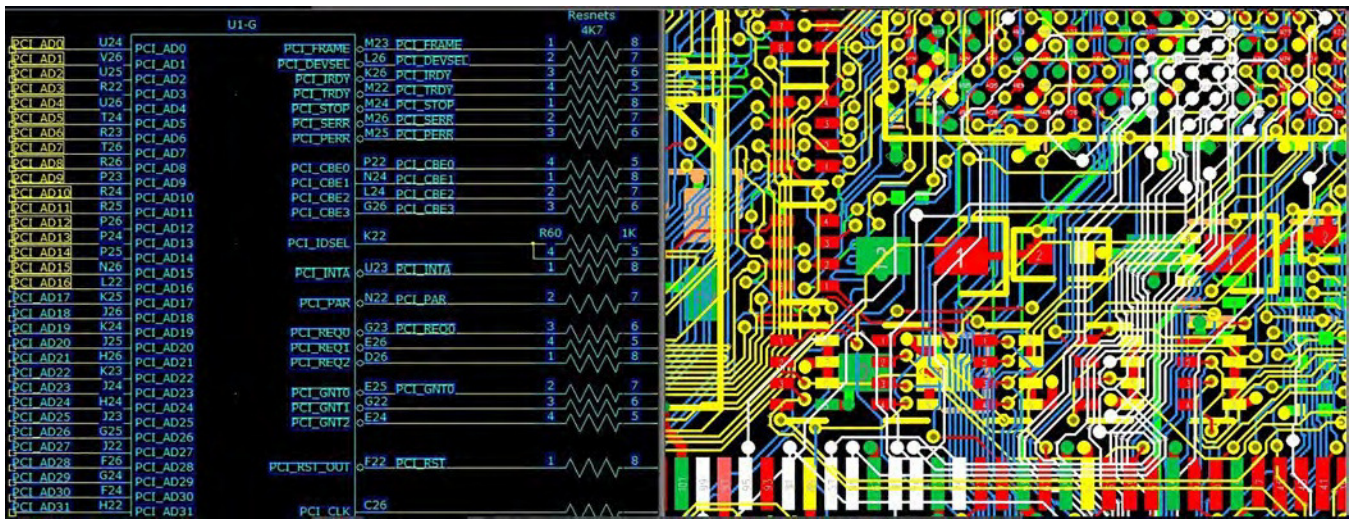


Figure 2: Cross-probing part of an address bus from schematic to router. (Source: Mentor Graphics, PADS)

On a multilayer PCB, critical signals should be routed on a stripline (inner layer) adjacent to a solid reference plane to reduce radiation. The spacing between the signal trace and return plane should be as small as possible to increase coupling and reduce loop area.

The three constraints to keep in mind include:

1. Making the mark to space ratio of the waveform equal because this eliminates all the even harmonics
2. Routing high-speed signals between the planes and fanout out close to the driver (200 mils), dropping to an inner layer and

route back up to the load again with a short fanout

3. Using the same reference plane (GND if possible) for the return signal because it reduces the loop area and radiation

As you can see from Figure 3, the trace routed on inner layer three exhibits between four to 10 dB less noise than the trace routed on the top layer. Note that there are radiating harmonics above 40 dB on the top layer routing. Also, high-frequency components radiate more readily because their shorter wavelengths are comparable to trace lengths, which act as antennas.

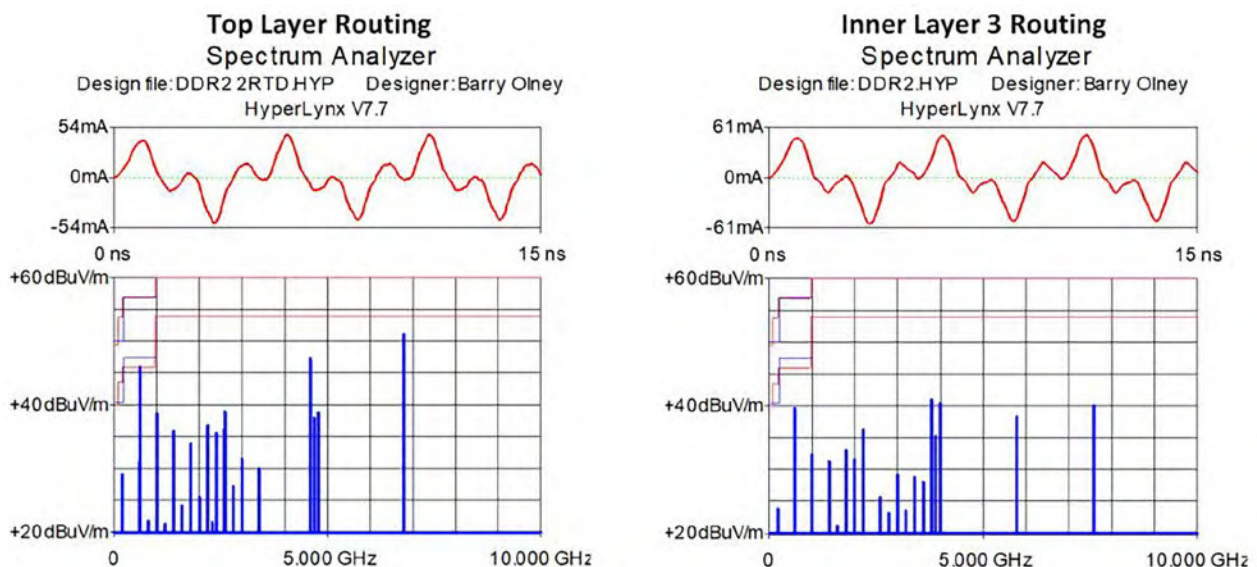


Figure 3: Comparison of signals routed on the top versus inner layer three. (Source: HyperLynx)

Consequently, although the amplitude of the harmonic frequency components decreases, as the frequency increases, the radiated frequency varies depending on the traces characteristics.

For a synchronous bus—providing the receiver waits sufficiently long enough for the crosstalk to settle—before sampling the bus, the crosstalk on data and address signals within each group has little impact on the signal quality at the receiver. This can be ensured by always making the clock or strobe the longest signal of a matched length group.

For a perfectly balanced differential signal, the radiation from one trace exactly cancels the radiation from the other as they are equal and opposite. However, a common-mode signal represents an average of the two signals in a pair. The radiation is identical on both traces, and therefore, does not cancel but instead reinforces. The transformation from differential to common-mode takes place on bends and non-symmetrical routing near via and pin obstructions. This also impacts the impedance of the pair. To minimize radiation and crosstalk, one must think explicitly about the common-mode component of the differential signal; skew creates this common-mode signal.

Arguably, the principal source of imbalance is time-delay skew between the two traces. The easiest way to minimize this skew is to match the electrical lengths and to correct any shift immediately after it arises by adding length (hence the delay) to the shorter trace.

VII. Analyze the Return Current Paths: All signal traces should be tightly coupled to a contiguous reference plane and have a clearly defined minimum loop inductance return current path.

High-speed design is not as simple as sending a signal from the driver to the receiver over an interconnect. Rather, one should also consider the presence and interaction of the power distribution network (PDN) and how and where the return current flows.

Generally, PCB designers take great care to ensure that critical signals are routed exactly to length from the driver to the receiving device pins, but they take little care of the return current path of the signal. Current flow is a

round trip, and the important issue is delay—not length. If it takes one signal longer for the return current to get back to the driver—around a gap in the plane for instance—then there will be skew between the critical timing signals. Return path discontinuities (RPDs) can create large loop areas that increase series inductance, degrading signal integrity and increasing crosstalk and electromagnetic radiation.

Small discontinuities, such as vias and non-uniform return paths on a bus, are becoming an important factor for the signal integrity and timing of high-speed systems. RPDs produce impedance discontinuities due to the local return inductance and capacitive changes. Impedance discontinuities create reflected noise, contribute to differential channel-to-channel noise, and may promote mode conversion. In the case of differential pairs, the transformation from differential-mode to common-mode typically takes place on bends, and asymmetrical routing near via and pin obstructions, but can also be caused by small changes in impedance due to RPDs.

Each signal layer should be adjacent to—and closely coupled to—a contiguous reference plane that creates a clear, uninterrupted return path and eliminates broadside crosstalk. As the layer count increases, this concept becomes easier to implement, but decisions regarding return current paths become more challenging.

Although power planes can be used as reference planes, ground is more effective as local stitching vias can be used for the return current transitions rather than stitching decoupling capacitors, which add inductance. This keeps the loop area small and reduces radiation. As the stackup layer count increases, so does the number of possible combinations of the structure. But, if one sticks to the basic rules, then the best-performing configurations are obvious.

Figure 4 shows the electric and magnetic fields emanating from a signal trace in both a microstrip and stripline configuration. Electric fields (blue) terminate when they come into contact with a solid plane while magnetic fields (red) are shielded by the planes, but the fringing fields still tend to radiate from the board edges.

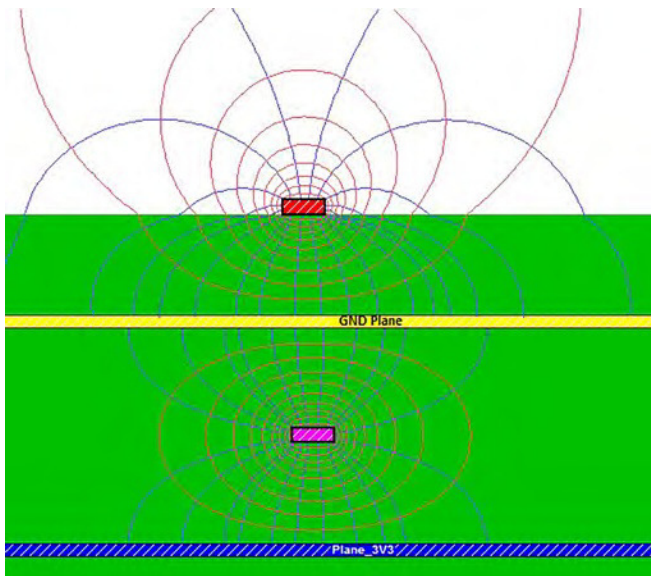


Figure 4: Microstrip and stripline electromagnetic fields. (Source: HyperLynx)

Unfortunately, return path discontinuities can never be totally eliminated, but we can take steps to minimize their impact significantly. As with PDN planning, it is all about inductance. If the return path loop area is increased in any way, then the inductance will also increase.

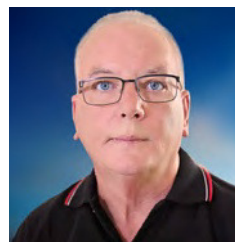
Key Points:

- Critical signals should be routed first with the precision they require
- It is important to understand the flow of the return current path of critical signals because these can influence the signal integrity and EMC
- Before starting placement and routing, detailed interconnect routing constraints should be established
- The most efficient approach to placement is to cross-probe between the schematic and the PCB/routing editor
- Critical signals should be routed on a stripline (inner layer) adjacent to a solid reference plane to reduce radiation
- The spacing between the signal trace and the return plane should be as small as possible to increase coupling and reduce loop area
- Timing can be assured and crosstalk ignored by always making the clock or strobe the longest signal of a matched length group of a synchronous bus

- One should consider the presence and interaction of the PDN and how and where the return current flows
- Current flow is a round trip, and the important issue is delay—not length
- RPDs produce impedance discontinuities due to the local return inductance and capacitive changes
- The transformation from differential-mode to common-mode typically takes place on bends and asymmetrical routing
- Each signal layer should be adjacent to—and closely coupled to—a contiguous reference plane, which creates a clear, uninterrupted return path and eliminates broadside crosstalk
- Although power planes can be used as reference planes, ground is more effective as local stitching vias can be used

Further Reading: “Beyond Design” Columns by Barry Olney

- [Common Symptoms of Common-Mode Radiation](#), *Design007 Magazine*, May 2018.
- [Crosstalk Margins](#), *Design007 Magazine*, July 2018.
- [The Dark Side—Return of the Signal](#), *The PCB Design Magazine*, August 2011.
- [The Dumping Ground](#), *The PCB Magazine*, August 2011.
- [Embedded Signal Routing](#), *The PCB Magazine*, September 2011.
- [Return Path Discontinuities](#), *The PCB Design Magazine*, April 2017.
- [Routing Techniques for Complex Designs](#), *The PCB Design Magazine*, January 2013.
- [Uncommon Sense](#), *The PCB Design Magazine*, August 2011.



Barry Olney is managing director of In-Circuit Design Pty Ltd (iCD), Australia, a PCB design service bureau that specializes in board-level simulation. The company developed the iCD Design Integrity software incorporating the iCD

Stackup, PDN, and CPW Planner. The software can be downloaded from www.icd.com.au. To read past columns or contact Olney, [click here](#).