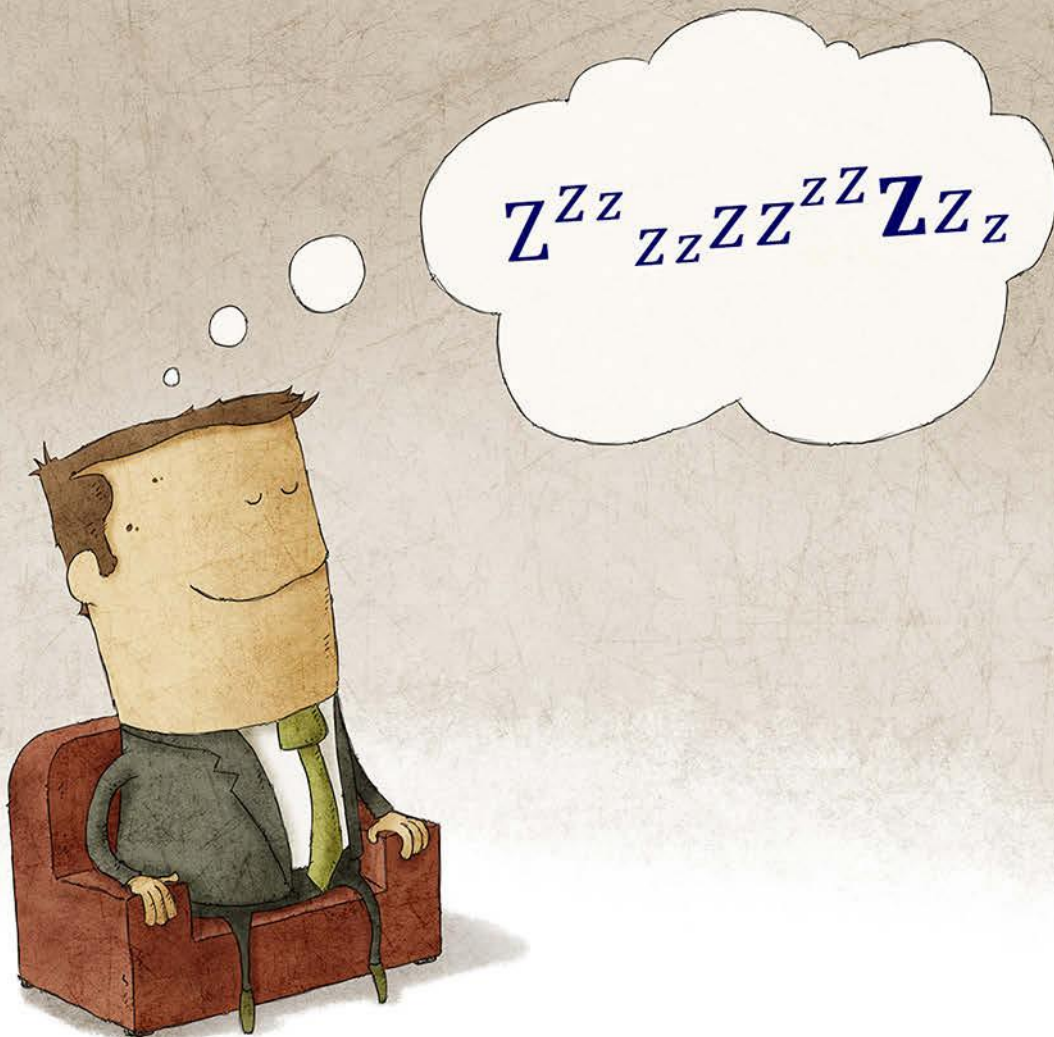


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10 Fundamental Rules of High-Speed PCB Design, Part 1

Beyond Design

by Barry Olney, IN-CIRCUIT DESIGN PTY LTD / AUSTRALIA

Over the years, I have focused on high-speed design, signal and power integrity, and EMC design techniques in a plethora of published technical articles—all of which have key points to consider and present a tremendous amount of information to absorb. In my next few columns, I will elaborate on ten of the most important considerations to embrace to achieve successful high-speed PCB designs that perform reliably to expectations.

Figure 1 lists the 10 fundamental rules of high-speed PCB design that I deem the most important to follow, although they may change after months of deliberation, like what happened with the laws of thermodynamics. The first established thermodynamic principle, which eventually became the second law, was formulated by Sadi Carnot in 1824. By the late 1800s, three laws of thermodynamics were clearly defined. However, in the 1930s—long after these three laws were already widely

accepted—Sir Ralph Fowler and E.A. Guggenheim felt that another law, which they saw as the foundation of earlier laws, should be incorporated. Hence, it was numbered the zeroth law. Thus, there is always room for one more at the top!

The 10 fundamental rules of high-speed PCB design are:

I. Establish Design Constraints

Always create a strategy for high-speed design requirements and set constraints based on pre-layout analyses or recommendations and guidelines prior to commencing the design.

II. Control the Impedance

Match the transmission line impedance to the driver and load. Create the stackup and define terminations to match the impedance.

III. Floor Plan the Placement Based on Connectivity

Place components by functionality and analog and digital groups to minimize interaction between different logic families and improve routability and timing.

IV. Define the Power Delivery Planes and Paths

Define the power/ground regions and plane layers. Partition (not split) the ground planes.

V. Optimize the Power Distribution Networks (PDNs)

Create a low AC impedance delivery path by optimizing the bypass and decoupling capacitors and mounting inductance and plane resonance from DC to the

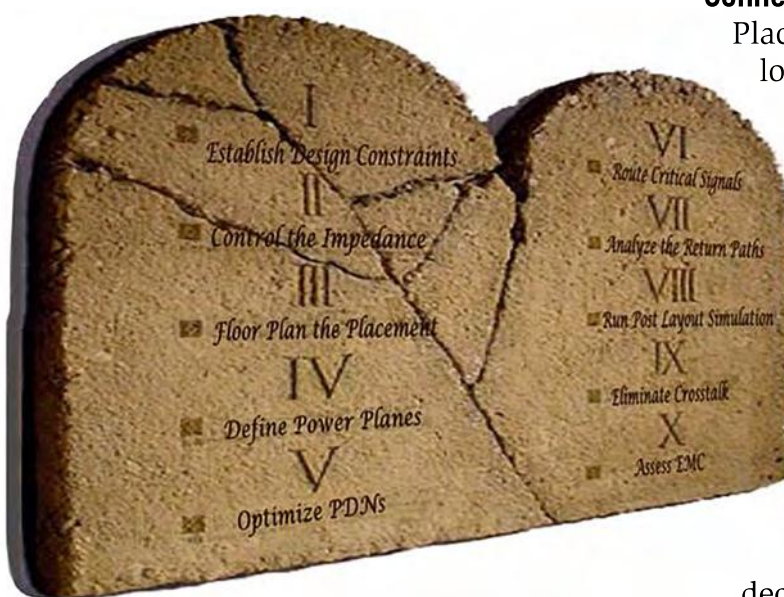


Figure 1: The 10 fundamental rules of high-speed PCB design.

maximum required frequency (including harmonics).

VI. Route the Board Based on Critical Signals

Adhere to the defined routing strategy. Clock signals should always have the longest delay of the group. Differential pairs should maintain constant impedance along the entire length.

VII. Analyze the Return Current Paths

All signal traces should be tightly coupled to a contiguous reference plane and have a clearly defined minimum loop inductance return current path.

VIII. Run the Post-Layout Simulation

Simulate critical signals and match signal propagation and timing. Check for signal ringing and eye jitter.

IX. Eliminate Crosstalk

Scan the board for possible crosstalk. Crosstalk can be coupled trace-to-trace on the same layer or broadside coupled by traces on adjacent layers.

X. Assess Electromagnetic Compliancy (EMC)

Control EM radiation at the source. Ensure that differential mode signals do not convert to common mode and eliminate any possible antennae.

Without further ado, I will begin with an elaboration of the first rule: Establish design constraints.

Complex, high-speed multilayer boards should be designed using a proven design methodology incorporating a pre-layout simulation before placing a single chip on the board. This includes reviewing component datasheets and design recommendations prior to the schematic capture. Simulation tools can be used to analyze various issues, such as reflections due to impedance discontinuities, crosstalk, signal attenuation, and PDN noise—all of which can impact interconnect performance.

Simulation of a PCB design after placement

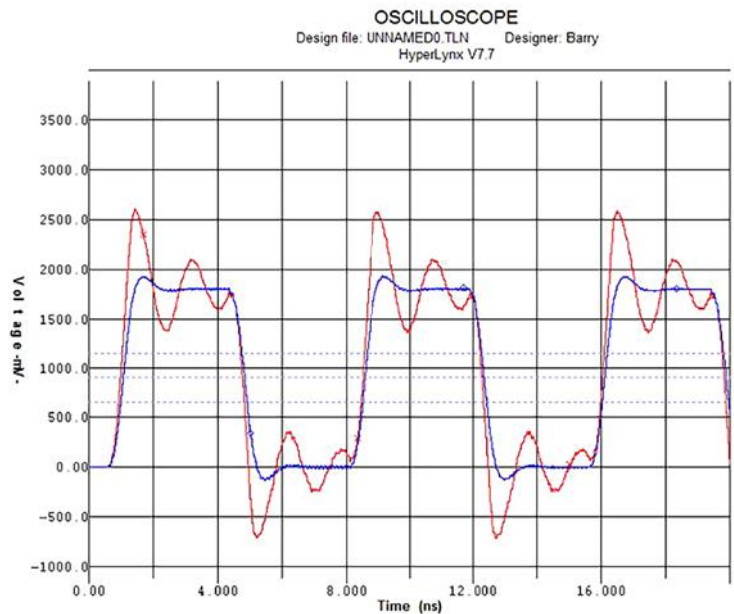


Figure 2: Pre-layout simulation with correction of clock ringing. (Source: HyperLynx)

and routing is recommended, but simulation early in the design phase is even better. Both are essential. Pre-layout analyses allow critical interface topologies, termination schemes, and I/O buffer selections to be defined and analyzed for synchronous, source-synchronous, and clock interfaces before placement and routing. Figure 2 depicts a simulated clock signal with (blue) and without (red) a series termination. Simulation opens one's eyes to what the circuitry is doing. It also leads to an enhanced perception of what might be a potential issue once the system is built.

There are multiple facets to pre-layout analyses, including:

- Stackup planning for controlled impedance, signal integrity, and crosstalk
- Dielectric material selection for high-frequency operation, manufacturing yield, and cost control
- I/O buffer and drive strength selection
- Topology optimization for signal integrity, timing, and EMC
- Series and parallel termination strategy
- Derived layout routing constraints, including trace width, spacing, and delay/length matching

- PDN analysis and decoupling capacitor optimization
- Signal integrity analysis to meet the design specifications with respect to noise margins, timing, skew, crosstalk, and signal distortion

Pre-layout simulations also allow a designer to identify and eliminate signal integrity, crosstalk, and EMC issues early in the design process. This is the most cost-effective way to design a board with fewer iterations. However, if you do not have access to simulation tools, then follow best practices from Design007 Magazine, IC manufacturers guidelines, etc.

While designs continue to increase in complexity and time-to-market remains critical, it is imperative to have a constraint system that is integral to your design flow. The constraints—based on a pre-layout simulation—manufacturing restrictions, and IC manufacturer’s recommendations and guidelines should flow from pre-schematic to PCB layout, routing, fabrication, and assembly.

Before starting placement and routing, detailed interconnect routing constraints should be established (Figure 3). Of course, these are based on the pre-layout simulation and impedance requirements. Firstly, determine the single-ended and differential impedance required for each technology used. Synchronous bus delay or length matching should be set up in the constraints editor along with differential pair rules and clearance between signal groups to prevent crosstalk while giving priority to critical signals.

Appropriate grouping and defining of net and constraint classes in the early stages of the design process significantly simplifies constraint definition and management. Grouped constraints can increase layout efficiency, reduce design time, and ultimately lower PCB design costs.

The prime objective behind setting constraints up front is to ensure that the design is going to perform to expectations. It is essential that the system can alert the designer to any errors as they occur. Interactive design rule

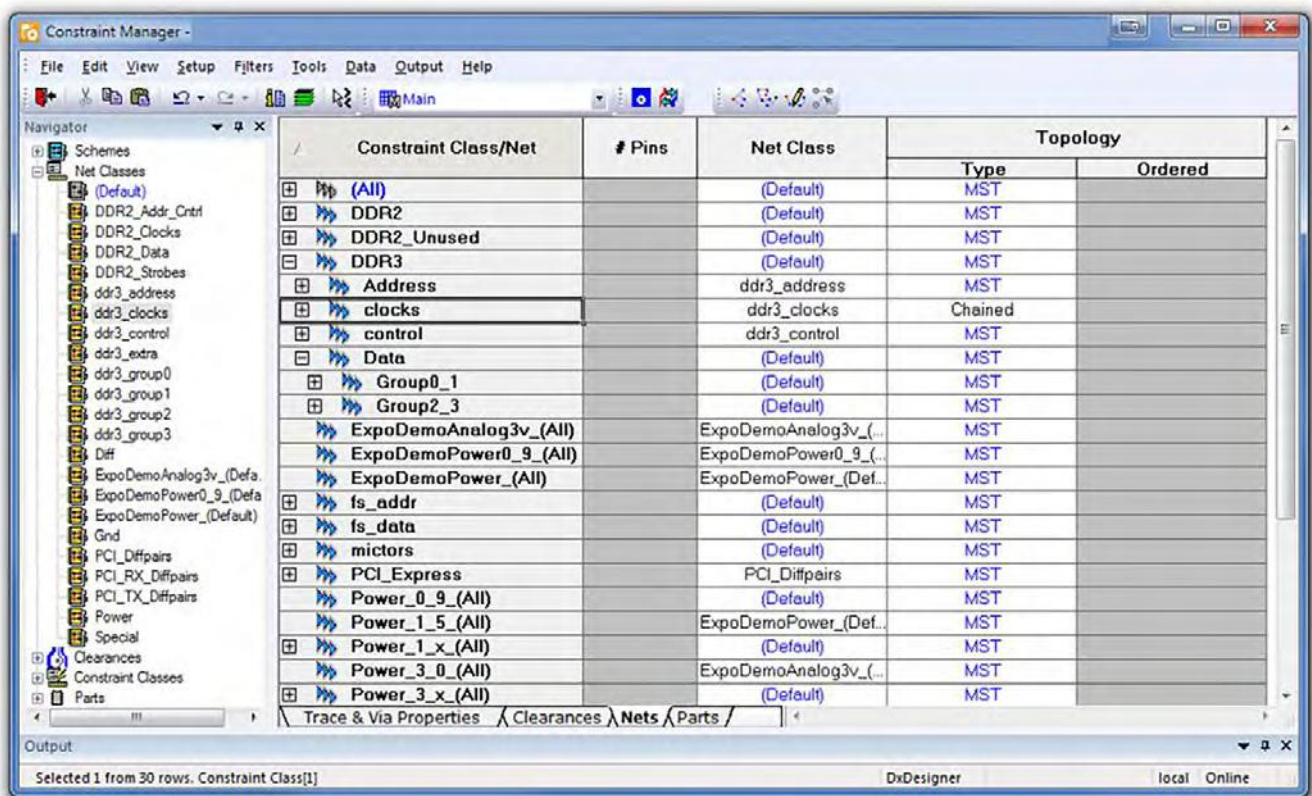


Figure 3: Typical high-speed design constraints. (Source: PADS Professional Constraint Manager)

checks (DRCs), which are adhered to throughout the design cycle, provide for an error-free, correct-by-construction design when carefully planned early in the design phase.

A robust constraint management system should be unified and integrated into the schematic and layout editors with cross-probing, including:

- Integrated topology-driven constraint definition
- Controlled impedance rules, including spacing and clearance to other nets
- Length or time-based constraints
- Electrical constraints with custom equation capability
- Physical trace and spacing rules (class-to-class rules, etc.)
- Region and technology rules
- Same net DRCs for advanced technologies (HDI)
- PCB fabrication, assembly, and testability rules (if required)

Although all designs are different, one should reuse existing rules where possible as a template to eliminate the need for re-entry of any common constraints. These include DDRx, PCIe, USB, SATA, Ethernet, differential pair rules, manufacturing requirements, etc. This also minimizes the possibility of input errors.

When constraints are defined at the beginning of the design process, designers can be confident that once the design phase is completed, the product will move through the production phases with fewer errors. A constraint management system that can check work in real time as the design process is executed provides reduced risk and peace of mind that the constraints will prevent the PCB designer from violating the rules set up front. Although we cannot plan for the unexpected, having a reliable constraint management system in place will ensure that the majority of issues are covered and will alert you if any unforeseen issues arise.

Stay tuned for next month's column that will continue to elaborate on the 10 fundamental rules of high-speed PCB design.

Key Points

- Simulation of a PCB design early in the design process is essential
- Pre-layout simulation leads to an enhanced perception of what might be a potential issue once the system is built
- It is imperative to have a constraint system that is integral to your design flow
- Detailed interconnect routing constraints should be established before starting placement and routing
- The prime objective behind setting constraints up front is to ensure that the design is going to perform to expectations
- Reuse existing rules when possible to eliminate the need for re-entry of any common constraints
- A constraint management system that can check work in real time as the design process is executed provides reduced risk and peace of mind

Further Reading

- [Beyond Design: Pre-Layout Simulation](#) by Barry Olney, The PCB Magazine, July 2012.
- [Beyond Design: Split Planes in Multilayer PCBs](#) by Barry Olney, The PCB Design Magazine, March 2015.
- [Beyond Design: Plane Crazy, Part 1](#) by Barry Olney, The PCB Design Magazine, December 2015.
- [Beyond Design: Interactive Placement and Routing Strategies](#) by Barry Olney, The PCB Design Magazine, December 2012.
- [Beyond Design: Controlling Emissions and Improving EMC](#) by Barry Olney, The PCB Design Magazine, August 2011.
- [5 Ways to Assess PCB Constraint Management Systems for High-Speed Designs](#), EMA Design Automation Blog.
- [Why impose PCB design constraints?](#) by Steve Hughes of Mentor, a Siemens Business.



Barry Olney is managing director of In-Circuit Design Pty Ltd (iCD), Australia, a PCB design service bureau that specializes in board-level simulation. The company developed the iCD Design Integrity software incorporating the iCD Stackup, PDN, and CPW Planner. The software can be downloaded from www.icd.com.au. To read past columns or contact Olney, [click here](#).