

My 100th Column

Beyond Design

by Barry Olney, IN-CIRCUIT DESIGN PTY LTD / AUSTRALIA

Believe it or not, this is my 100th “Beyond Design” column. The editors at I-Connect007 are a great group to work with. I eagerly await each month’s magazine release to see how creative the team have been with editing, laying out, and producing my column.

I-Connect007 was founded in 1999 and is now the industry’s longest-running electronics media portal. Personal development and continued education are so important—especially in a relatively new and ever-changing industry where designers are continually pushing the envelope. And with its line-up of three online magazines—Design007 (featuring Flex007), PCB007, and SMT007—I-Connect007 provides the latest information from industry experts.

My first “Beyond Design” column on ground pours was published online in 2011 ^[1]. Over the years, I think that I only missed publishing one month when I was on vacation. I’ll

have to work on that lazy streak! When I was first approached to write a regular column, I thought that I might be able to convert my course on advanced design for SMT, which I had been presenting throughout Australia and New Zealand since 1994, into a number of segments. However, I never envisaged reaching the 100 mark.

“Beyond Design” focuses on high-speed PCB design, signal and power integrity, and EMC design techniques. To wrap-up my 100th column, I look back over the past 99 columns and reflect on what I believe to be the Top 10 most enlightening for high-speed PCB designers, counting down in reverse order of preference.

10. The Dumping Ground

Ground planes in a multilayer PCB allow the designer to ground anything, anywhere, without having to run multiple tracks, the net



needing grounding being routed directly to the ground plane on another layer. However, this is a simplistic approach. One should also consider the presence and interaction of the power distribution network (PDN) and how and where the return current flows. A logic schematic diagram masks details crucial to the operation of unintentional signal pathways vital to your understanding of signal performance, crosstalk, and electromagnetic emissions.

When you plan your stackup, be aware of which plane(s)—either power or ground—will be the return path for your critical signals, and ensure there is an unobstructed return path. The best way to think of this is to imagine routing a return trace adjacent to each signal trace on the reference plane. Where will the current flow, and is it unobstructed? The reference plane adjacent to each signal layer allows the return current to flow as closely as possible to the signal trace reducing inductance and loop area.

9. PDN and Capacitor Selection, Parts 1 and 2

This two-part column focused on capacitor selection and three alternative approaches to analyzing the PDN:

1. Target frequency
2. One-value capacitor per decade
3. Optimized value capacitor

The target frequency approach has been traditionally used. This method targets a precise frequency and is used to reduce AC impedance as well as EMI within a specific band. The alternatives of using either a one-value capacitor per decade or many optimized capacitors are used in an attempt to level out the AC impedance at the desired impedance over a broad frequency band (Figure 1).

8. Signal Integrity, Parts 1-3

As system performance increases, the PCB designer's challenges become more complex. The impact of lower core voltages, high frequencies, and faster edge rates has forced us into the high-speed digital domain. But in reality, these issues can be overcome by experience and good design techniques. If you don't currently have the experience, then listen up. This three-part series on signal integrity covered the following topics:

- How advanced IC fabrication techniques have created havoc with signal quality and radiated emissions
- The effects of crosstalk, timing, and skew on signal integrity
- Where most designer's go wrong with signal integrity, and how to avoid the common pitfalls

7. Plane Crazy, Parts 1 and 2

A high-speed digital PDN must provide a

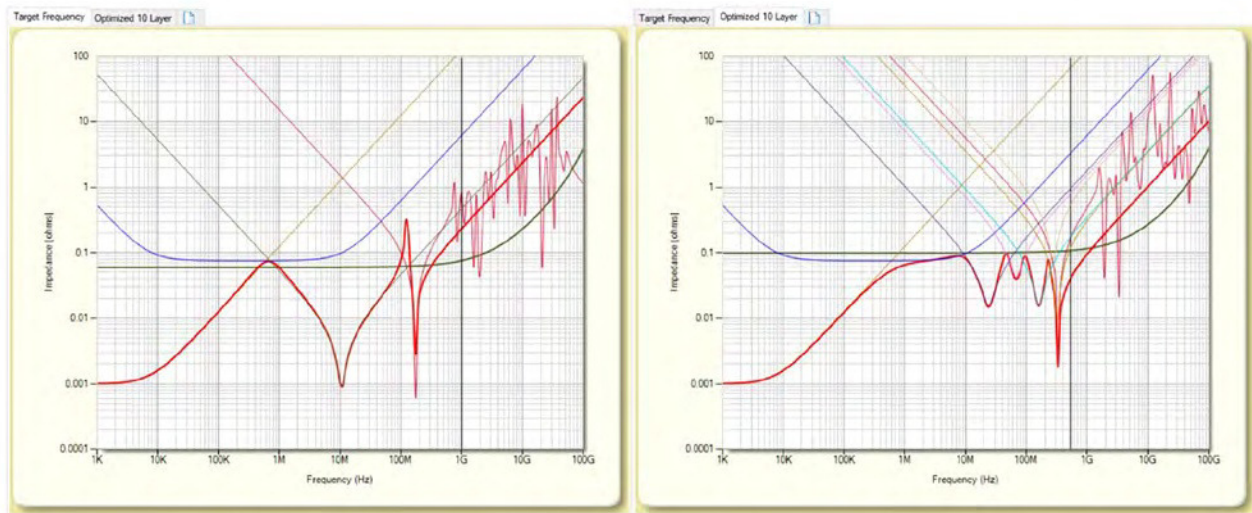


Figure 1: Target frequency vs. optimized value approaches (iCD PDN Planner).

low-inductance, low-impedance path between all ICs on the PCB that need to communicate. To reduce the inductance, you must also minimize the loop area enclosed by the current flow. The most practical way to achieve this is to use power and ground planes in a multilayer stackup. In this two-part column, I looked at the alternatives to planes, why planes are used for high-speed design and the best combination for your application.

6. DDR3/4 Fly-by Topology: Termination and Routing

DDR3/4 fly-by topology is similar to daisy-chain or multi-drop topology but has very short stubs to each memory device in the chain to reduce the reflections. The advantage of fly-by topology is that it supports higher-frequency operation and improves signal integrity and timing on heavily loaded signals. If you are employing high-frequency DDR4, then the bandwidth of the channel needs to be as high as possible. However, with today's extremely fast edge rates, the sequencing of the stubs and the end termination and the associate load can make a measurable difference in signal quality. In this column, I explored how best to route DDR3/4 fly-by topology (Figure 2).

For more background reading, check out my two-part series on "PCB Design Techniques for DDR, DDR2, and DDR3" [2].

5. Microstrip Coplanar Waveguides

The classic coplanar waveguide (CPW) is formed by a microstrip conductor strip separated from a pair of ground plane pours, all on the same layer affixed to a dielectric medium. In the ideal case, the thickness of the dielectric is infinite. But in practice, it is thick enough so that electromagnetic fields die out before they get out of the substrate. A variant of the coplanar waveguide is formed when a ground reference plane is provided on the opposite side of the dielectric. This is referred to as a conductor-backed or grounded CPW. CPWs have been used for many years in RF and microwave design as they reduce radiation loss at extremely high frequencies compared to traditional microstrip. As edge rates continue to rise, they are coming back in vogue. In this column, I described how conformal field theory could be used to model the electromagnetic effects of microstrip coplanar waveguides.

4. The Dark Side: Return of the Signal

All PCB designers should be aware of the impact of crosstalk on signal integrity. As signal traces come into close proximity of an aggressor signal, part of that signal is unintentionally electromagnetically coupled into the victim trace as noise. I have mentioned before that current flow is a roundtrip; the current must return back to the source to complete the loop.

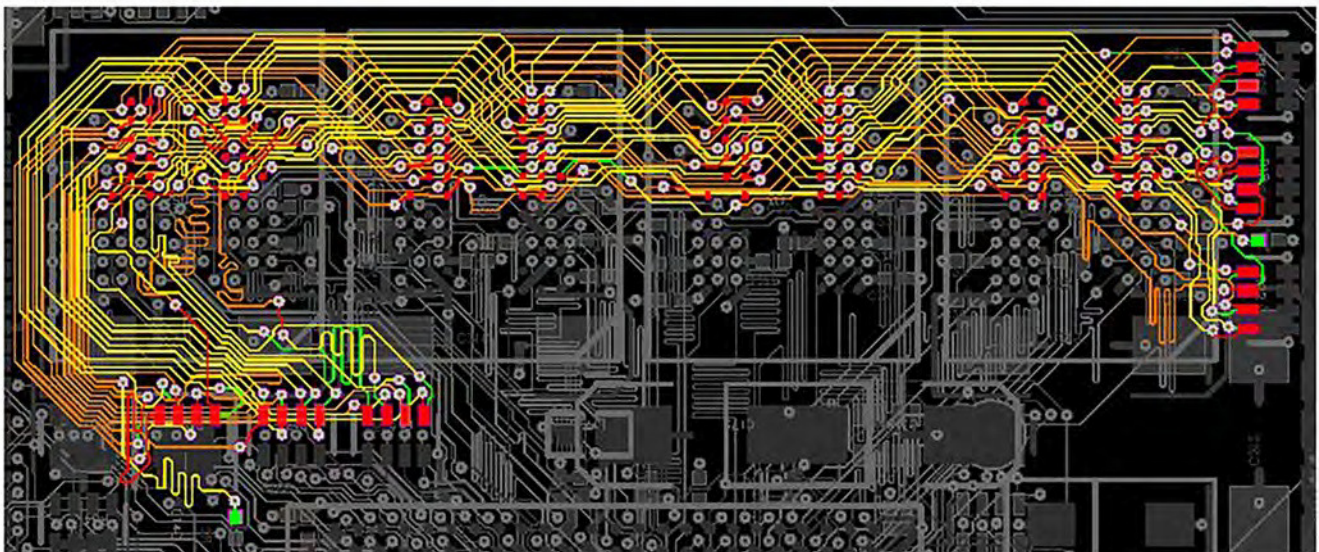


Figure 2: Fly-by topology for clock, address, command, and control routing.

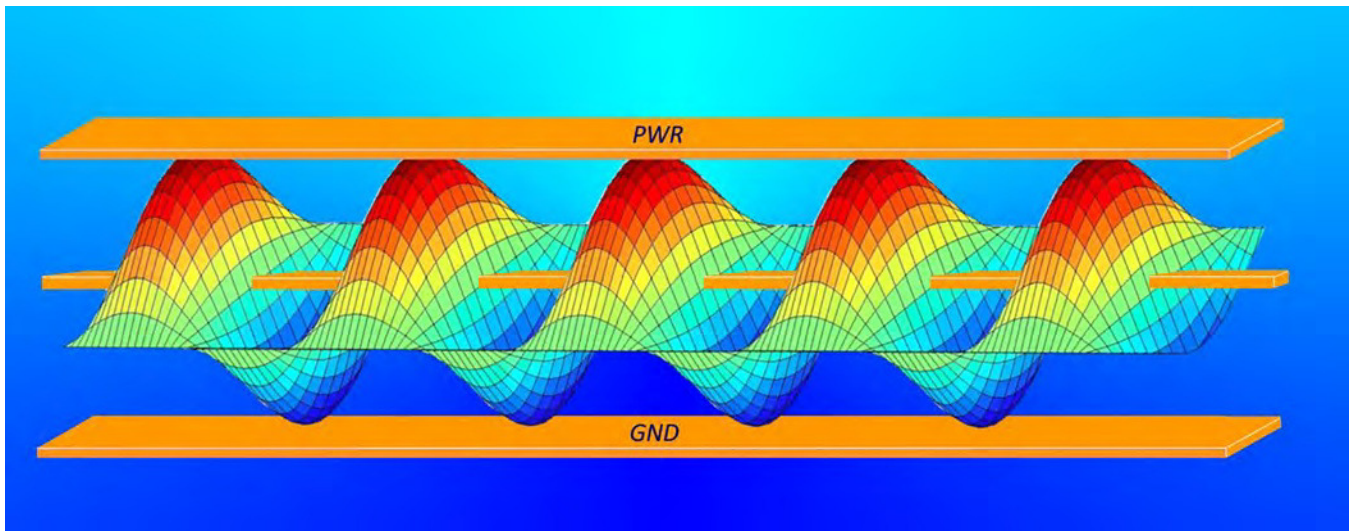


Figure 3: Digital signals travel as a wave of electromagnetic energy in a multilayer PCB.

So, what about crosstalk in the return path of the reference planes as the current weaves its way back through the expansive wasteland of copper? This column followed my previous column “Return-Path Discontinuities”^[3] and elaborated on crosstalk in the unseen “dark side” of the signal.

3. Next-gen PCBs: Substrate-integrated Waveguides

As PCB transmission frequencies head toward 100 GHz and beyond, the current mainstream PCB technology—the copper interconnect—is reaching its performance threshold. Ultimately, it is dielectric loss, copper roughness, and data transfer capacity that are the culprits. However, the biggest performance restriction for PCB interconnects is the size of the conductor. Metallic waveguides are a better option compared to traditional transmission lines, but they are bulky, expensive, and non-planar in nature.

Recently, substrate integrated waveguides (SIW) structures have emerged as a viable alternative and are ideally suited to the high-speed transmission of electromagnetic waves. SIW are planar structures fabricated using two periodic rows of PTH vias or slots connecting the top and bottom copper ground planes of a dielectric substrate. In this column, I reviewed the substrate integrated waveguide and its incorporation with the microstrip transmission line.

2. Stackup Planning, Parts 1-5

Design methodologies change over time, particularly in the ways to simulate electromagnetic fields and return current paths. In my first four columns on stackup planning, I described the traditional stackup structures that use a combination of signal and power/ground planes. But to achieve the next level in stackup design, one needs to not only consider the placement of signal and plane layers in the stackup but also visualize the electromagnetic fields that propagate the signals through the substrate. Part 5 covers all of the latest concepts in stackup design (Figure 3).

1. The 10 Fundamental Rules of High-speed PCB Design, Parts 1-5

Over the years, in a plethora of published technical articles, I have focused on high-speed design, signal and power integrity, and EMC design techniques. All of these have key points to consider and present a tremendous amount of information to absorb. In this five-part series, I reflected on the 10 most important considerations to embrace to achieve a successful high-speed PCB design that performs reliably to expectations. These 10 golden rules should be the prime checklist for all high-speed PCB designers (Figure 4).

Moving forward, does anyone have a suggestion for the theme of my 101st column? How about “Signal Integrity 101”? Feel free suggest

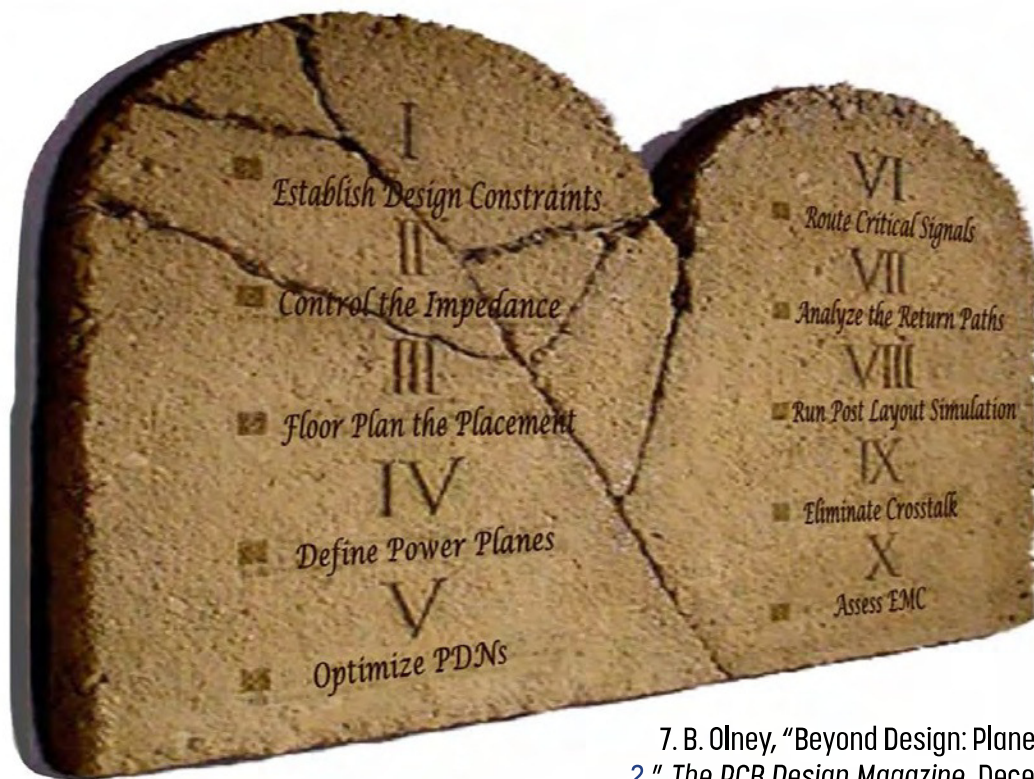


Figure 4: The 10 fundamental rules of high-speed PCB design.

a topic through the link on my [columnist page](#) (left side). **DESIGN007**

Editor's Note: The references correspond with the numbered headings, and the further reading suggestions correspond with the superscripts throughout the column.

References

1. B. Olney, "Beyond Design: The 10 Fundamental Rules of High-speed PCB Design, [Part 1](#), [Part 2](#), [Part 3](#), [Part 4](#), and [Part 5](#)," *Design007 Magazine*, September, October, November, and December 2018, and January 2019.
2. B. Olney, "Beyond Design: Stackup Planning, [Part 1](#), [Part 2](#), [Part 3](#), [Part 4](#), and [Part 5](#)," *The PCB Design Magazine*, June 2015, July 2015, August 2015, and October 2015, and *Design007 Magazine*, July 2019.
3. B. Olney, "Beyond Design: Next-Gen PCBs—Substrate-Integrated Waveguides," *The PCB Design Magazine*, November 2017.
4. B. Olney, "Beyond Design: The Dark Side—Return of the Signal," *The PCB Design Magazine*, May 2017.
5. B. Olney, "Beyond Design: Microstrip Coplanar Waveguides," *The PCB Design Magazine*, March 2017.
6. B. Olney, "Beyond Design: DDR3/4 Fly-by Topology—Termination and Routing," *Design007 Magazine*, June 2018.

7. B. Olney, "Beyond Design: Plane Crazy, [Part 1](#) and [Part 2](#)," *The PCB Design Magazine*, December 2015 and January 2016.

8. B. Olney, "Beyond Design: Signal Integrity, [Part 1](#), [Part 2](#), and [Part 3](#)," *The PCB Design Magazine*, October, November, and December 2014.

9. B. Olney, "Beyond Design: PDN and Capacitor Selection, [Part 1](#) and [Part 2](#)," *The PCB Design Magazine*, December 2013 and January 2014.

10. B. Olney, "Beyond Design: The Dumping Ground," *The PCB Magazine*, August 2011.

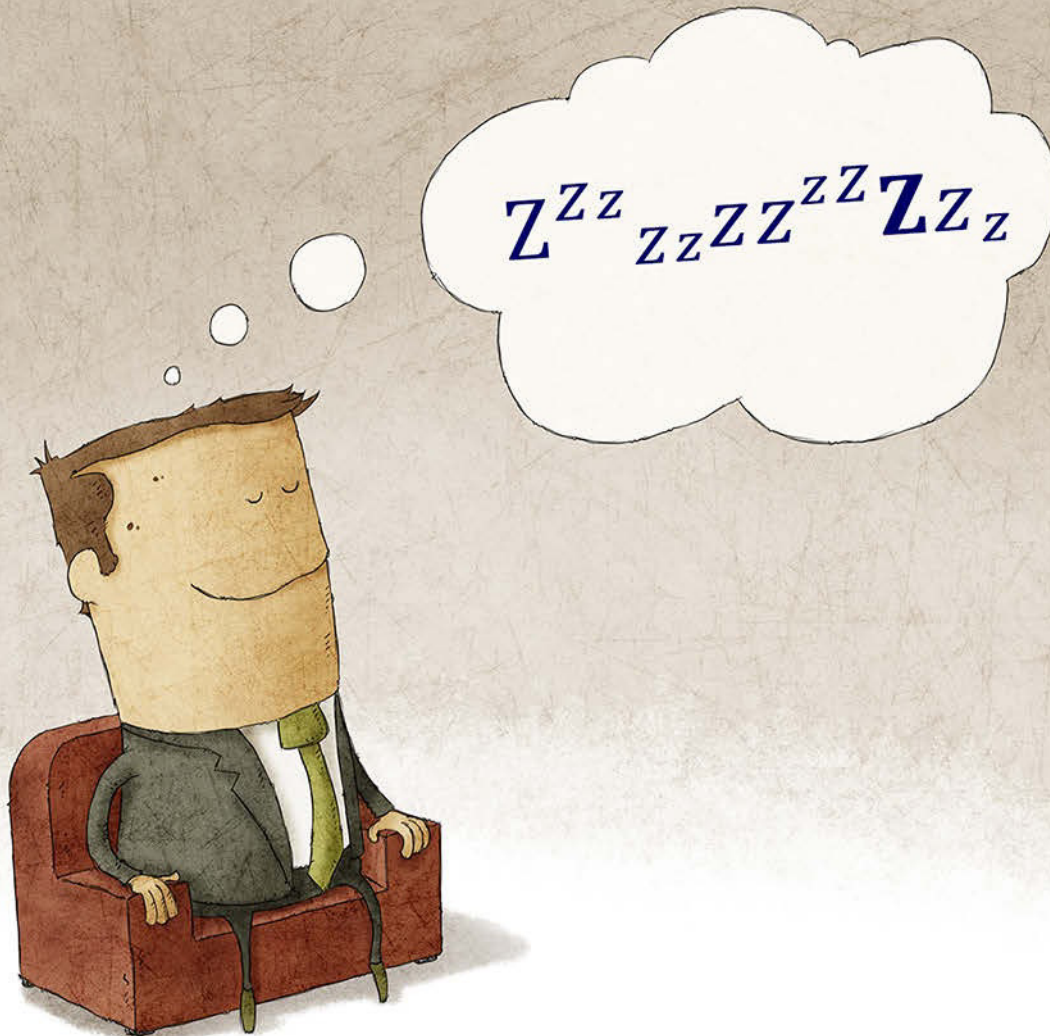
Further Reading

1. B. Olney, "Beyond Design: Ground Pours: To Pour or Not to Pour," I-Connect007 online, 2011.
2. B. Olney, "Beyond Design: PCB Design Techniques for DDR, DDR2, and DDR3, [Part 1](#) and [Part 2](#)," *The PCB Design Magazine*, May and June 2011.
3. B. Olney, "Beyond Design: Return-Path Discontinuities," *The PCB Design Magazine*, April 2017.



Barry Olney is managing director of In-Circuit Design Pty Ltd. (iCD), Australia, a PCB design service bureau that specializes in board-level simulation. The company developed the iCD Design Integrity software incorporating the iCD Stackup, PDN, and CPW Planner. The software can be downloaded www.icd.com.au. To read past columns or contact Olney, [click here](#).

We **DREAM** Impedance!



Did you know that two seemingly unrelated concepts are the foundation of a product's performance and reliability?

- Transmission line impedance and
- Power Distribution Network impedance

DISCOVER MORE

iCD software quickly and accurately analyzes impedance so you can sleep at night.

iCD Design Integrity: Intuitive software for high-speed PCB design.

"iCD Design Integrity software features a myriad of functionality specifically developed for PCB designers."

– Barry Olney

