The Dumping Ground

by Barry Olney | In-Circuit Design Pty Ltd | Australia

This Application Note discusses best practices for selecting reference planes and routing pairs for high speed designs on multilayer boards.

Wikipedia definition: "A *ground plane* in a PCB assembly is a layer of copper that appears to most signals as an infinite ground potential. This helps reduce noise and helps ensure that all integrated circuits within a system compare different signals' voltages to the same reference potential. Ground planes can also be placed on adjacent layers to power planes creating a large parallel plate capacitor that helps filter the power supply."

"It also serves to make the circuit design easier, allowing the designer to ground anything without having to run multiple tracks; the component needing grounding is routed directly to the ground plane on another layer." Hmm! Well actually, that may be the case with DC or very low frequency and analog circuits but certainly not when we are talking high speed design.

In a DC circuit the return current takes the path of least resistance –sort of like pouring a bucket of water on the ground. The water takes the path of least resistance and follows the troughs to the lowest point. But at high speed (> 30 MHz) the return current takes the path of least inductance which just happens to be the reference plane (either ground or power) directly below the trace.

Fig. 1 Ground is not a sheet of copper.

The ground plane is not a dumping ground for unwanted signal returns. Fig. 1 is an example of what the ground plane would look like if one reference plane was used for a number of signal layers.

The return currents follow the path of least inductance with the streams of electrons crossing over each other. Although this is probably immeasurable, one would assume that there would be some sort of detrimental interaction (crosstalk) between these streams. This is why each signal layer should have a dedicated reference plane.

One point that always amazes me: Designers generally take great care to ensure that matched length signals are routed exactly to length from the driver to the DRR2 device pin, but take no care of the return path of the signal. Current flow is a 'round trip.' If it takes one signal longer for the return current to get back to the driver (around a gap in the plane for instance) then there will be skew between the critical timing signals.

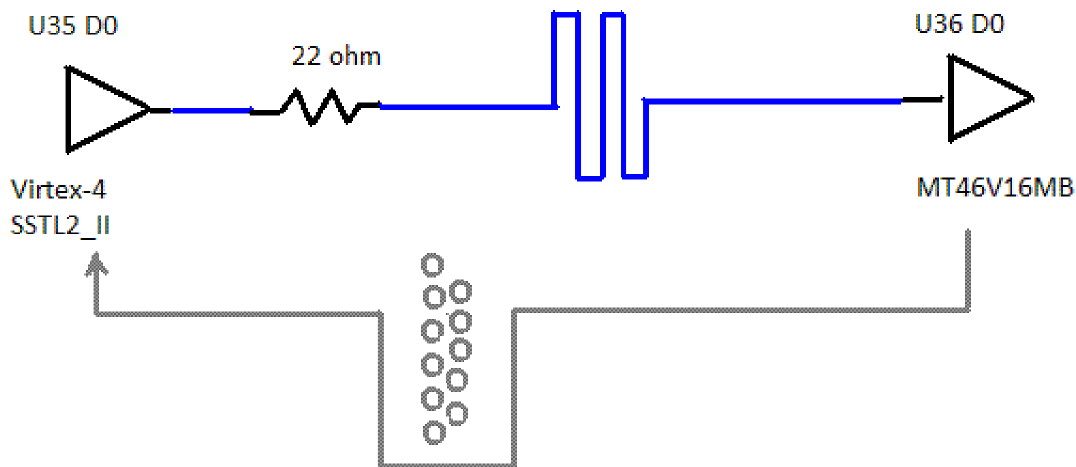

Fig.3 The return current for a Data signal diverts around the connector antipads in the plane

When you plan your stackup, be aware of which plane(s) (either power or ground) will be the return path for your critical signals and make sure there is an unobstructed return path. The best way to think of this is to imagine routing a return trace adjacent to each signal trace on the reference plane – where is the best place for the current to flow and is it unobstructed? The reference plane adjacent to each signal layer allows the return current to flow as closely as possible to the signal trace reducing inductance and loop area.

The ideal high speed stackup is illustrated in Fig. 4. This eight layer stackup is commonly used for DDR2 & DDR3 designs as each signal layer has a reference plane on both sides thus avoiding crosstalk from adjacent signal layers and providing a clear return path for the current. This stackup has been built with the ICD Stackup Planner (download from www.icd.com.au).

Layer pairs for routing the memory are 1 & 3 (Data lanes & Strobes) and 1 & 6 (Address bus & clocks) using GND for both reference planes. 90 ohm differential USB signals can be routed on layer 3. Single ended 50 ohm on any layer and differential 100 ohm signals on any other layer.

ICD STACKUP PLANNER – www.icd.com.au 6/29/2011

UNITS: MIL

Total Board Thickness: 61.2

Layer		Material	Dielectric		Copper	Trace		Current	Impedance	Edge Coupled	Broadside Coupled	
Number	Name	Type	Constant	Thickness	Thickness	Clearance	Width	(Amps)	Characteristic(Zo)	Differential(Zdiff)	Differential(Zdbs)	Description
		Dielectric	3.3	0.5								Soldermask
1	Top	Conductive			1.4	8	4	0.31	53.53	99.99		Signal
		Dielectric	4.3	3								Prepreg
2	GND	Conductive			1.4							Plane
		Dielectric	4.3	8								Core
3	Inner 3	Conductive			1.4	12	5	0.37	51.96	90.66		Signal
		Dielectric	4.3	8								Prepreg
4	VCC	Conductive			1.4							Plane
		Dielectric	4.3	12								Core
5	GND	Conductive			1.4							Plane
		Dielectric	4.3	8								Prepreg
6	Inner 6	Conductive			1.4	12	4	0.31	56.4	98.4		Signal
		Dielectric	4.3	8								Core
7	VDD	Conductive			1.4							Plane
		Dielectric	4.3	3								Prepreg
8	Bottom	Conductive			1.4	8	4	0.31	53.53	99.99		Signal
		Dielectric	3.3	0.5								Soldermask

Fig. 4 Ideal 8 layer Stackup

If possible we should use the one reference plane for the return path. In this case we have used GND but the return path can be any reference plane ground or power. Choosing layer 2 for the reference plane allows the return current to initially follow the signal path on the top surface of the GND plane then crossing over to the bottom surface through the via antipad so it is as close as possible to the signal path. This is called the 'skin effect'. At high frequencies current doesn't flow evenly through the entire cross section of the copper plane but is more concentrated at the surface. Because of the skin effect, at high frequencies, the current can't pass through the copper plane (the plane acts more like a hollow conductor) and has to go from top to bottom surface through the via antipad.

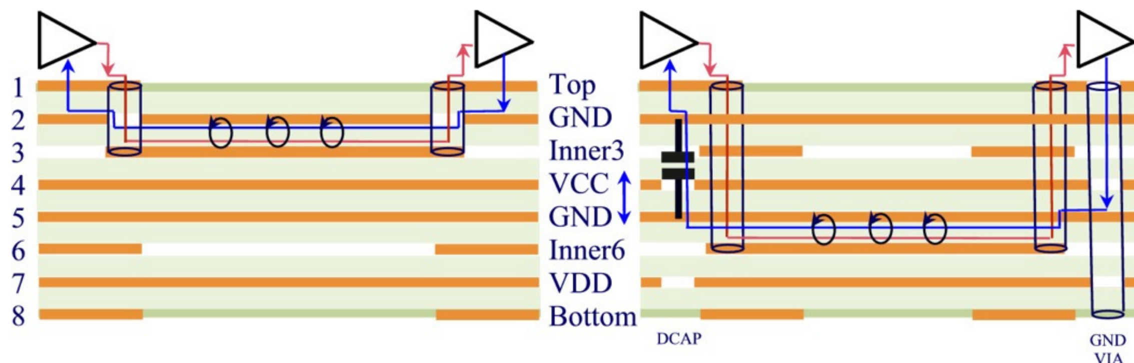

Fig. 4 Signal and return paths for routing pairs

Routing pairs 1 & 3 – Data lanes & Strobes

The signal fans out from the driver on layer 1 to 3 and then is routed on layer 3 over to the load and then back up to layer 1. The return current drops to the top of the GND plane then swaps to the bottom surface through the via antipad coupling closely to the signal on layer 3 then back up through the via to the top surface of GND and then back to the source.

Routing pairs 1 & 6 – Address bus, Clocks & Commands

The signal fans out from the driver on layer 1 to 6 and then is routed on layer 6 over to the load and then back up to layer 1. The return current goes to the nearest GND stitching via to jump to the GND plane on layer 5. It then swaps from top surface to bottom surface of GND through the via antipad coupling closely to the signal on layer 6 then will try to find a path back to the source via the nearest GND via.

An interesting scenario is if we swap plane layers 4 & 5 (VCC & GND). In this case, VCC would be used for the reference plane in the drawing to the right. So how will the return current get back to the driver from layer 5? It's a shame that electrons can't fly. The current will have to go to the nearest DCAP between VCC and GND to jump layers. If there is no DCAP nearby, this may be as far away as the power supply creating a huge loop area and hence radiation (EMI). So it is important to place a DCAP close to every via to aid the return signal. That reminds me of another one of my wise sayings: "Where ever there is room – place another DCAP". You can never have too many.

In order to change reference planes:

- If there are multiple ground planes then place a stitching via as close as possible to each signal via.
- If power planes are also used as the reference plane then place DCAP's as close as possible to each signal via.

Also, please keep in mind that high speed signals should not be routed on the outer layers. Embedding the signals between the planes (on layers 3 & 6) reduces the radiation by at least 10 dB. So, fanout from the driver and drop to the internal signal layer routing up to the load through a short stub.

In conclusion, the PCB Designer must route the signal trace and also mentally route the return path in order to keep flight times tight, crosstalk low and radiation (EMI) to a minimum. The best way to think of this is to imagine routing a return trace adjacent to each signal trace on the reference plane – where is the best place for the current to flow and is it unobstructed?

References:

PCB Design Techniques for DDR, DDR2 & DDR3 – Barry Olney
Advance Design for SMT – Barry Olney
Design for EMC – Barry Olney
Electromagnetic Compatibility Engineering – H. Ott
High Speed Design – H. Johnson
The ICD Stackup Planner can be downloaded from www.icd.com.au

All consideration has been taken to ensure that this Application Note is accurate, based on the information and data available. The liability of In-Circuit Design Pty Ltd is limited to correcting any unforeseen errors and revising the Application Note to meet the specified requirements. In no event shall In-Circuit Design Pty Ltd be liable for indirect, special, incidental, punitive or consequential damages including but not limited to whether occasioned by the act, breach, omission, default or negligence of In-Circuit Design Pty Ltd, its employees, contractors and subcontractors, and shall include without limitation, loss of business, revenue or profits, loss of use or data, loss of savings or anticipated savings, loss of investments, loss of goodwill, loss of reputation or cost of capital or loss of extra administrative cost, or economic loss, whether or not foreseeable, and arising out of or in connection with this Application Note. All trademarks are registered trademarks of their respective owners. E&OE