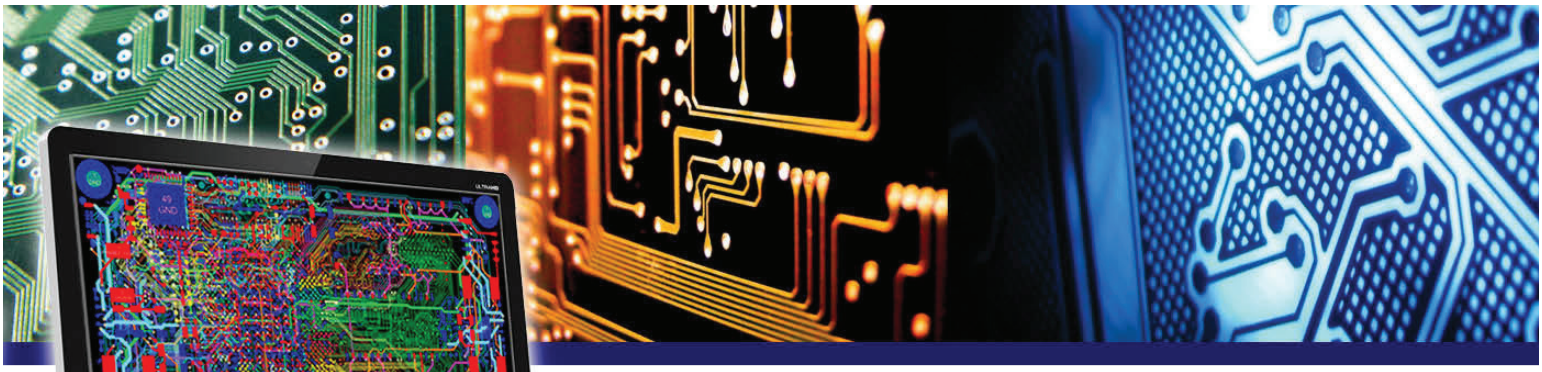

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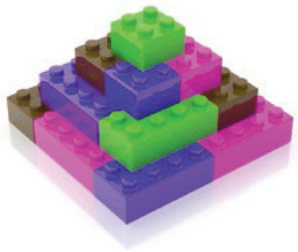
Stackup Planning, Part 2



by Barry Olney
IN-CIRCUIT DESIGN PTY LTD

In Part 1 of the Stackup Planner series, I looked at how the stackup is built, the materials used in construction and the lamination process. And I set out some basic rules to follow for high-speed design. It is important keep return paths, crosstalk and EMI in mind during the design process. Part 2 follows on from this with definitions of basic stackups starting with four and six layers. Of course this methodology can be used for higher layer count boards—36, 72 layers and beyond.

Four-Layer Stackup

A four-layer board is probably not the most practical configuration for high-speed design. Although it does have the advantage, over double sided boards, of using planes for the distribution of power and ground and the planes also act as the return current path for signals. Microstrip traces tend to radiate emissions and this configuration should be avoided in preference to embedding the critical signals using a higher layer count configuration. On the other hand, if you intend mounting the four-layer board, completely shielded, in a metal box then this configuration may be acceptable.

Since all (most) stackups are symmetrical, then it is best to just work on just the top half of the stackup to begin with—this halves the construction time. Stackups are generally symmetrical, with even amounts of copper about the center, in order to prevent the board from warping during fabrication and during the reflow process. If one half has more copper, then it will cool at a slower rate thus warping the board.

The layer selection process is a follows:

1. With four layers, two planes are placed in the center of the substrate. One ounce (1.4 mil) copper is typical for plane layers.
2. Prepreg material separates the signal layers from the planes and this should be as thin as possible in order to achieve close coupling.
3. Solder mask is generally added to the outer layers. This will reduce the impedance by a few ohms.

In Figure 1, the virtual materials yield a 54.44 ohm signal ended and 96.82 ohm differential impedance. This is close enough (to 50 ohms). Now let's fine-tune this stackup by inserting real dielectric materials and then adjust the variables to get the desired impedance.

The ICD Stackup Planner's Dielectric Materials Library contains over 16,700 commonly used core, prepreg and solder mask materials, arguably the most comprehensive list of material properties ever compiled. Using the exact materials that are stocked by your fabricator can increase accuracy by up to 5%. So before you start this process, it is best to consult your fab

2 Layer | 4 Layer | 6 Layer | 8 Layer | 10 Layer | 12 Layer | 14 Layer | 16 Layer | 18 Layer

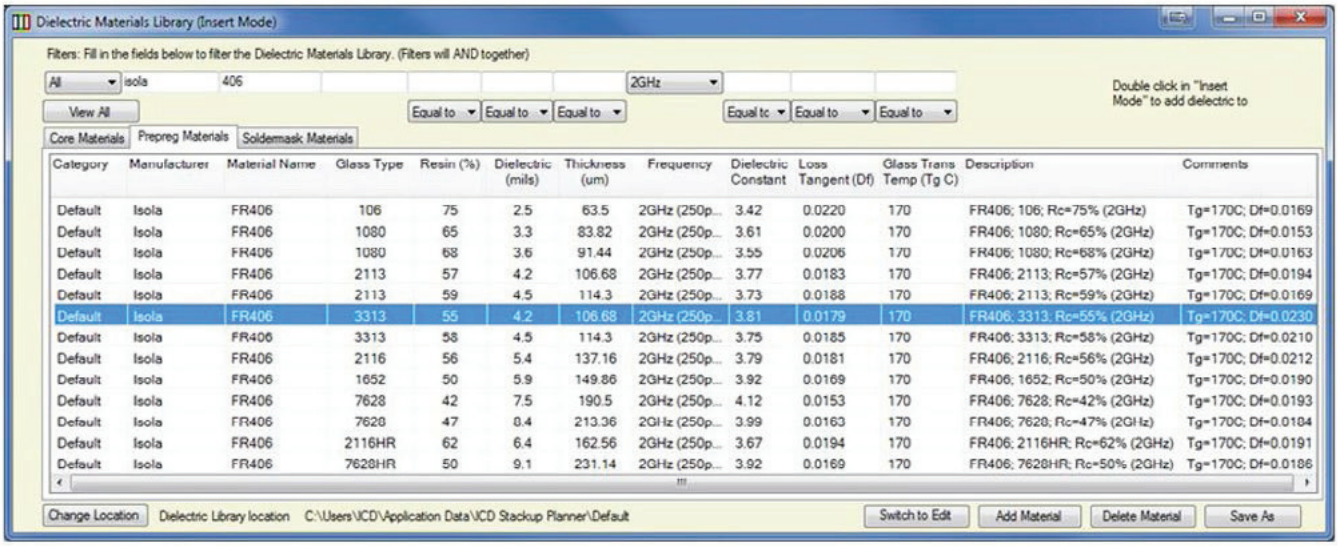
UNITS: mil — 6/1/2015 — Total Board Thickness: 10.8 mil

Differential Pairs > 50/100 ohms

Layer No.	Via	Description	Layer Name	Material Type	Dielectric Constant	Dielectric Thickness	Copper Thickness	Trace Clearance	Trace Width	Current (Amps)	Characteristic Impedance (Zo)	Edge Coupled Differential (Zdiff)	Broadside Coupled Differential (Zdbs)
		Soldermask		Dielectric	3.3	0.5							
1	8	Signal	Top	Conductive			1.4	12	12	0.69	54.44	96.82	
		Prepreg		Dielectric	4.3	8							
2		Plane	GND	Conductive			1.4						

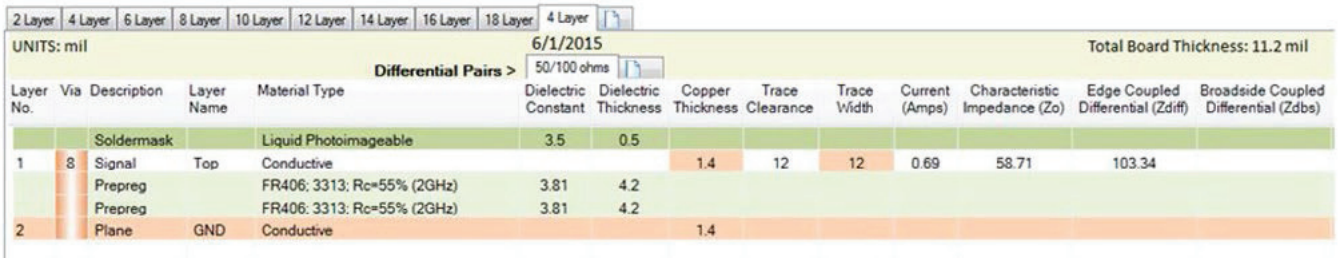
Figure 1: The top half of the four-layer stackup using virtual materials.

STACKUP PLANNING, PART 2 *continues*



Category	Manufacturer	Material Name	Glass Type	Resin (%)	Dielectric (mils)	Thickness (um)	Frequency	Dielectric Constant	Loss Tangent (Df)	Glass Trans Temp (Tg C)	Description	Comments
Default	Isola	FR406	106	75	2.5	63.5	2GHz (250p...	3.42	0.0220	170	FR406; 106; Rc=75% (2GHz)	Tg=170C; Df=0.0169
Default	Isola	FR406	1080	65	3.3	83.82	2GHz (250p...	3.61	0.0200	170	FR406; 1080; Rc=65% (2GHz)	Tg=170C; Df=0.0153
Default	Isola	FR406	1080	68	3.6	91.44	2GHz (250p...	3.55	0.0206	170	FR406; 1080; Rc=68% (2GHz)	Tg=170C; Df=0.0163
Default	Isola	FR406	2113	57	4.2	106.68	2GHz (250p...	3.77	0.0183	170	FR406; 2113; Rc=57% (2GHz)	Tg=170C; Df=0.0194
Default	Isola	FR406	2113	59	4.5	114.3	2GHz (250p...	3.73	0.0188	170	FR406; 2113; Rc=59% (2GHz)	Tg=170C; Df=0.0169
Default	Isola	FR406	3313	55	4.2	106.68	2GHz (250p...	3.81	0.0179	170	FR406; 3313; Rc=55% (2GHz)	Tg=170C; Df=0.0230
Default	Isola	FR406	3313	58	4.5	114.3	2GHz (250p...	3.75	0.0185	170	FR406; 3313; Rc=58% (2GHz)	Tg=170C; Df=0.0210
Default	Isola	FR406	2116	56	5.4	137.16	2GHz (250p...	3.79	0.0181	170	FR406; 2116; Rc=56% (2GHz)	Tg=170C; Df=0.0212
Default	Isola	FR406	1652	50	5.9	149.86	2GHz (250p...	3.92	0.0169	170	FR406; 1652; Rc=50% (2GHz)	Tg=170C; Df=0.0190
Default	Isola	FR406	7628	42	7.5	190.5	2GHz (250p...	4.12	0.0153	170	FR406; 7628; Rc=42% (2GHz)	Tg=170C; Df=0.0193
Default	Isola	FR406	7628	47	8.4	213.36	2GHz (250p...	3.99	0.0163	170	FR406; 7628; Rc=47% (2GHz)	Tg=170C; Df=0.0184
Default	Isola	FR406	2116HR	62	6.4	162.56	2GHz (250p...	3.67	0.0194	170	FR406; 2116HR; Rc=62% (2GHz)	Tg=170C; Df=0.0191
Default	Isola	FR406	7628HR	50	9.1	231.14	2GHz (250p...	3.92	0.0169	170	FR406; 7628HR; Rc=50% (2GHz)	Tg=170C; Df=0.0186

Figure 2 : Isola FR406 4.2 mil prepreg.



Layer No.	Via	Description	Layer Name	Material Type	Dielectric Constant	Dielectric Thickness	Copper Thickness	Trace Clearance	Trace Width	Current (Amps)	Characteristic Impedance (Zo)	Edge Coupled Differential (Zdiff)	Broadside Coupled Differential (Zdbs)
		Soldermask		Liquid Photoimageable	3.5	0.5							
1	8	Signal	Top	Conductive			1.4	12	12	0.69	58.71	103.34	
		Prepreg		FR406; 3313; Rc=55% (2GHz)	3.81	4.2							
		Prepreg		FR406; 3313; Rc=55% (2GHz)	3.81	4.2							
2		Plane	GND	Conductive			1.4						

Figure 3: Virtual materials replaced by Isola FR406 material.

shop and ask what materials they have in stock. For this example, I will use Isola FR406 which is a common low-cost material.

1. Select an 8 mil prepreg. Since 8 mil is not available in the Isola FR406 range, I will select 4.2 mil and add two sheets together. Multiple prepregs are often combined to achieve the desired thickness.
2. Edit the solder mask and select a typical liquid photoimageable material.

Now that all the virtual materials have been replaced with the stocked items, you can see that the single ended impedance is a bit out. The differential is 103.34 ohms.

1. Adjust the trace width to get closer to 50 ohms, then adjust the trace clearance to get 100

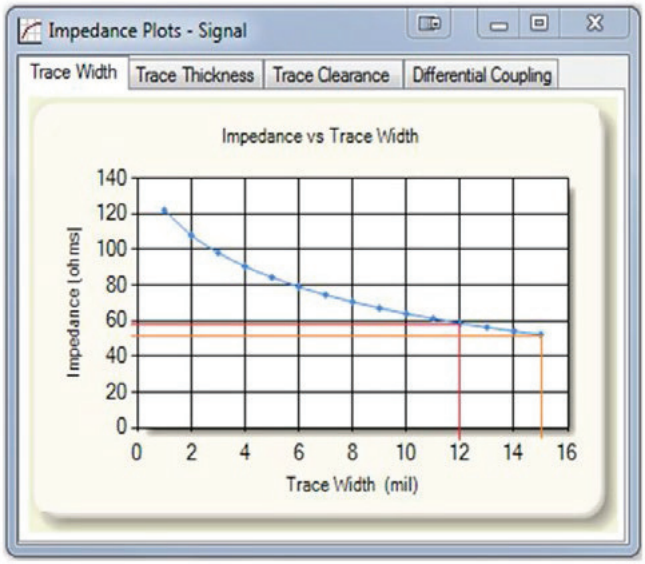


Figure 4: Impedance plots are used to determine correct trace width for 50 ohms.

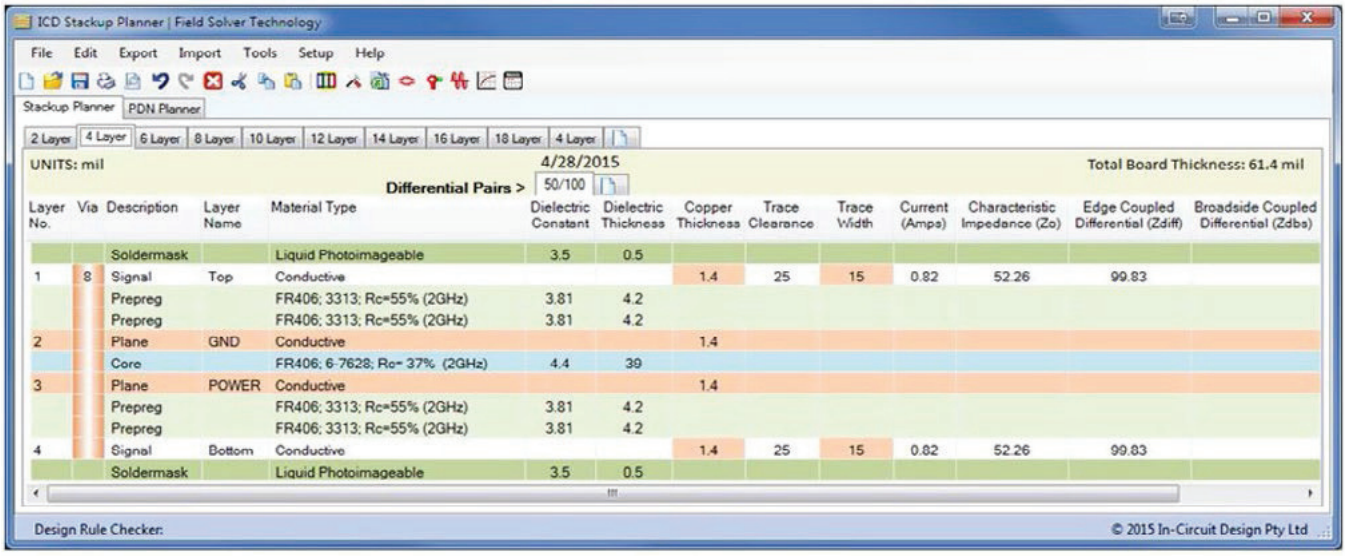


Figure 5: Completed four-layer stackup with ~ 50/100 ohms impedance.

ohms differential. In the Figure 4 impedance plot, you can see that a ~15 mil trace width is required to achieve ~50 ohms impedance.

2. Since the stackup is symmetrical, this top section of the stackup can be mirrored to create the entire stackup of Figure 5. You need to find a center core of appropriate thickness to beef-up the total board thickness to about 62 mils. A 39 mil core is selected from the Isola FR406 range to achieve this.

Now in this case, I was not able to tightly couple the ground and power planes because the center core had to be used to beef-up the total board thickness. However, to improve the EMC performance of a four-layer board, it is best to space the signal layers as close as possible to the planes, and use a large core between the power and ground plane keeping the overall thickness of the substrate to ~ 62 mils. For high-speed applications, you could reduce the trace width to say 4 mils and prepreg thickness to ~3 mils as shown in the six-layer stackup of Figure 7. This is the most cost-effective and most overlooked way to improve the performance of a four-layer PCB.

There are three advantages to this configuration:

1. The signal loop areas are smaller and therefore produce less differential mode radiation. Tight coupling between the signal and reference planes can amount to ~10 dB reduction in the trace loop radiation compared a stackup with equally spaced layers.
2. This also reduces the plane impedance (inductance) hence reduces the common-mode radiation from the cables connected to the board.
3. And, tight coupling will also decrease the crosstalk between traces.

Six Layer Stackup

Generally a six-layer board is created by adding two more signal layers between the planes of the standard four layer configuration. This has a huge advantage, in that embedding high-speed signals between the planes can reduce electromagnetic radiation by up to 10 dB. Embedding signals between the planes also reduces susceptibility to radiation, as well as providing ESD protection. So, not only do we prevent noise from being radiated, but we also reduce the possibility of being affected by an external source.

Figure 6, illustrates the dramatic difference of radiated emissions from high-speed signals routed on the outer microstrip layers (left) compared to those routed on the embedded inner stripline layers (right). You can see a notable 10

STACKUP PLANNING, PART 2 *continues*

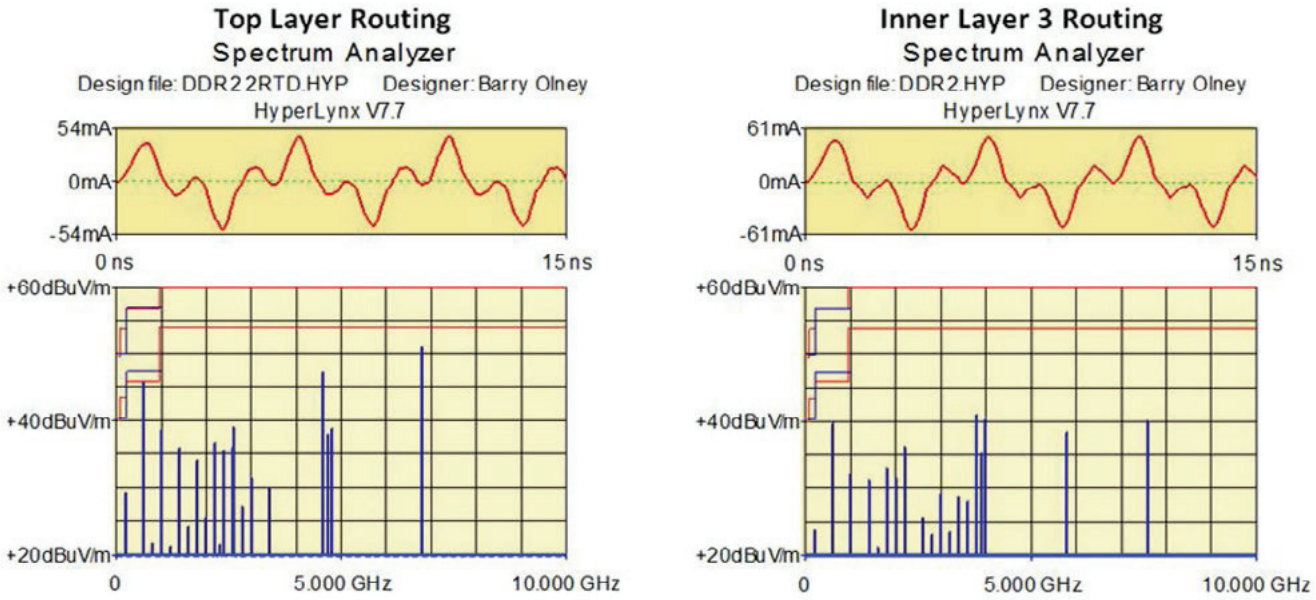


Figure 6: Comparison of radiated emissions from outer and inner layer routing.

dB reduction of emissions. This is enough, in this case, to get the board past the FCC Class B, electromagnetic compliancy.

There are four constraints to keep in mind:

1. Keep the mark-to-space ratio of the waveform equal, as this eliminates all the even harmonics.
2. Route high-speed signals out from the center of the board, where possible, as any radiation will be in the opposite direction and will tend to cancel.
3. Route high-speed signals between the planes, fanout out close to the driver (200 mils) dropping to an inner plane and route back up to the load again with a short fanout.
4. Use the same reference plane for the return signals as this reduces the loop area and hence radiation.

Figure 7 illustrates a six-layer stackup using Isola 370HR 2GHz material which is a commonly used product. This stackup configuration provides many advantages:

1. 1080 glass style prepreg is used for the microstrip outer layers. With just 2.8 mil thickness, this material provides close coupling between the outer signal and ground (GND).
2. The GND plane is used for the common reference—return path—for layers 1 & 3 and VCC for layers 4 & 6.
3. The signal loop areas are small and therefore produce less differential mode radiation.
4. The center is beefed-up by combining five sheets of 7628 material. This provides a total of 40 mils separation between the inner signal layers which reduces any broadside coupling that may occur. Also, routing these layers orthogonally will help reduce coupling.
5. EMI is reduced by routing the high-speed signal on layers 3 & 4 between the planes.

One minor disadvantage of this (and the previous four-layer) configuration is that there is not significant planar capacitance as the planes are separated by beefing-up the center core/prepreg. Therefore, the decoupling must be carefully selected to overcome this limitation. This is where a PDN Planner comes into play—a prelayout PDN analysis can import the stackup and evaluate the capacitance of the planes prior

STACKUP PLANNING, PART 2 *continues*

2 Layer | 4 Layer | 6 Layer 370 hr | 8 Layer | 10 Layer | 12 Layer | 14 Layer | 16 Layer | 18 Layer | 4 Layer

UNITS: mil — 6/1/2015 — Total Board Thickness: 59.2 mil

Differential Pairs > 50/100 ohms

Layer No.	Via	Description	Layer Name	Material Type	Dielectric Constant	Dielectric Thickness	Copper Thickness	Trace Clearance	Trace Width	Current (Amps)	Characteristic Impedance (Zo)	Edge Coupled Differential (Zdiff)	Broadside Coupled Differential (Zdbs)
		Soldermask		Dielectric	3.3	0.5							
1	8	Signal	Top	Conductive			1.4	8	4	0.31	53.95	100.85	
		Prepreg		370HR; 1080; Rc= 64% (2GHz)	3.89	2.8							
2		Plane	GND	Conductive			1.4						
		Core		370HR; 1-2116; Rc=47% (2GHz)	4.2	4							
3		Signal	Inner 3	Conductive			1.4	12	4	0.31	55.27	100.16	107.94
		Prepreg		370HR; 7628; Rc= 50% (2GHz)	4.16	8							
		Prepreg		370HR; 7628; Rc= 50% (2GHz)	4.16	8							
		Prepreg		370HR; 7628; Rc= 50% (2GHz)	4.16	8							
		Prepreg		370HR; 7628; Rc= 50% (2GHz)	4.16	8							
		Prepreg		370HR; 7628; Rc= 50% (2GHz)	4.16	8							
4		Signal	Inner 4	Conductive			1.4	12	4	0.31	55.27	100.16	107.94
		Core		370HR; 1-2116; Rc=47% (2GHz)	4.2	4							
5		Plane	VCC	Conductive			1.4						
		Prepreg		370HR; 1080; Rc= 64% (2GHz)	3.89	2.8							
6		Signal	Bottom	Conductive			1.4	8	4	0.31	53.95	100.85	
		Soldermask		Dielectric	3.3	0.5							

Figure 7: Six-layer stackup using Isola 370HR 2GHz material.

to fabrication. From this, one can approximate the required decoupling and adjustments can then be made to compensate.

In Figure 8, you can see that the lack of planar capacitance creates high AC impedance (0.38 ohms) at 275 MHz. In this case, more decoupling is required around 400 MHz. It may just be a matter of exchanging the 10nF capacitors for 1nF in order to bring the "V" curve, created by the capacitors, up in frequency. The plane area could also be adjusted to move the curve up or down in frequency in order to position the resonant frequency of the planes spot on the 400 MHz fundamental—this is a trial-and-error process that should be done before layout.

Over the years of analyzing customer boards, I have seen many variations of the four and six layer configurations in order to try and achieve the most cost-effective design. But realistically, adding a couple more layers is not expensive and provides more real estate for routing which will in turn yield a high-quality product with less crosstalk, and better EMC. Next month, I will look at higher layer-count boards, particularly 8-layer and 10-layer stackups that are preferred for high-speed applications.

Points to Remember

- A four-layer board has the advantage of using planes for the distribution of power and ground (GND) to the ICs on both sides of the board and the planes also act as the return current path for signals.
- Four-layer configuration boards should be avoided (unless completely shielded) as the microstrip traces tend to radiate.
- Since all stackups are symmetrical, then it is best to work on just the top half of the stackup to begin with—this halves the construction time.
- Six-layer boards have a huge advantage, over four layers, in that embedding high-speed signals between the planes can reduce electromagnetic radiation by up to 10dB.
- One minor disadvantage of four and six layer configurations is that there is no significant planar capacitance as the planes are separate by beefing up the center core/prepreg.
- A prelayout PDN analysis can import the stackup and evaluate the capacitance of the planes prior to fabrication. Adjustments can then be made to the decoupling to compensate.

STACKUP PLANNING, PART 2 *continues*

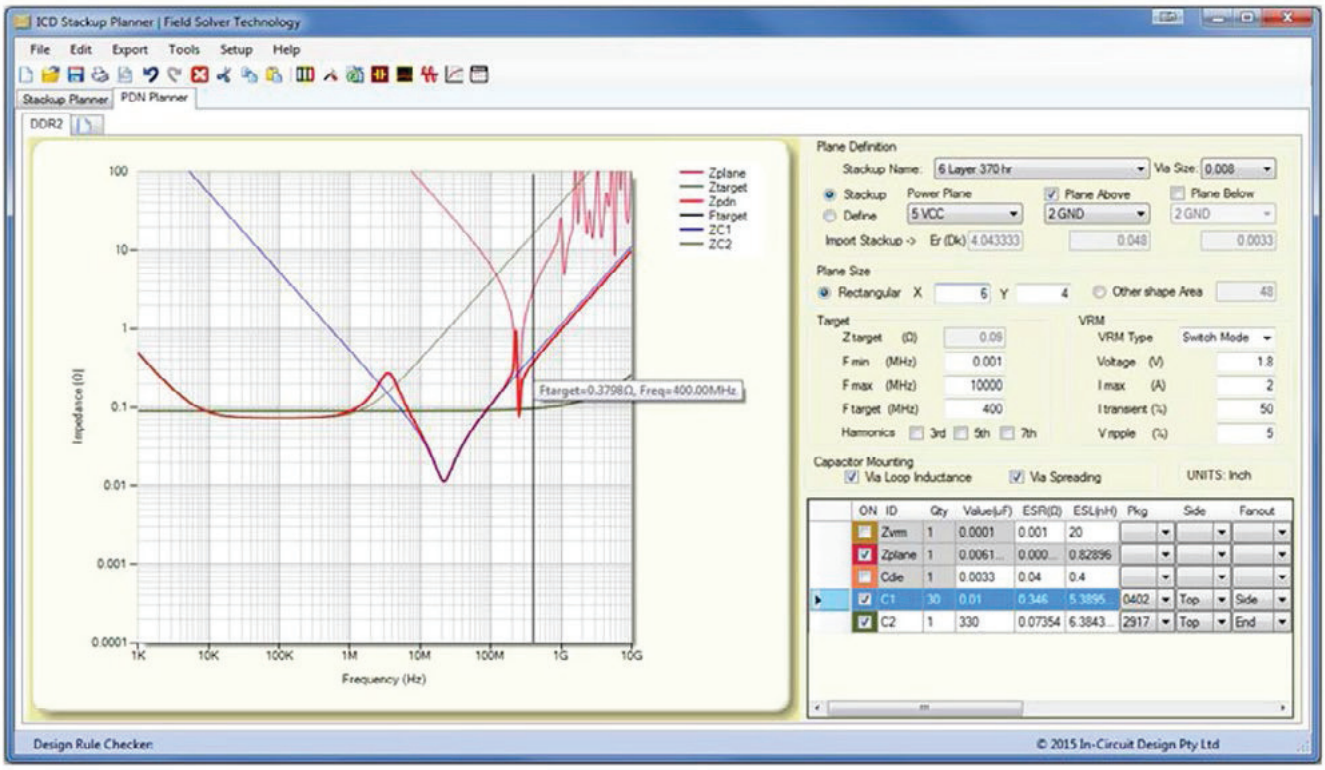


Figure 8: PDN analysis of the six-layer Isola 370HR stackup with decoupling.

References

1. Barry Olney Beyond Design columns: Material Selection for SERDES Design, Material Selection for Digital Design, The Perfect Stackup for High-Speed Design, and Embedded Signal Routing.

2. Henry Ott: Electromagnetic Compatibility Engineering.

3. The ICD Stackup and PDN Planner, visit www.icd.com.au.

Barry Olney is managing director of In-Circuit Design Pty Ltd (ICD), Australia. The company developed the ICD Stackup Planner and ICD PDN Planner software, is a PCB Design Service Bureau and specializes in board level simulation. To read past columns, or to contact Olney, click here.

New Lithium Ion Battery is Safer, Tougher, and More Powerful

South Korean researchers at the Center for Self-assembly and Complexity, Institute for Basic Science, have created a new lithion ion battery from a porous solid which greatly improves its performance.

The new battery is built from pumpkin-shaped molecules called cucurbit[6]uril (CB[6]) which are organized in a honeycomb-like structure.

What makes this new technique exciting is that it is a new method of preparing a solid lithium electrolyte which starts as a liquid, but no post-synthetic modification or chemical treatment is needed.