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# Skewed Again

by Barry Olney

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When skew needs to be adjusted, it is best done at either end of the differential pair.

In this way, the coupling and signal quality of the remainder of the pair is maintained.

Differential signaling is a method of transmitting serial, high-speed, complementary signals down a pair of coupled transmission lines. The equal and opposite nature of the differential pair means that demand on the power distribution network (PDN) is less than for a similar, single-ended data path. And, since external interference tends to affect both signals equally, the noise is cancelled providing high immunity to common mode electromagnetic interference compared to single-ended transmissions. But that is assuming the pair are perfectly balanced and terminated correctly. Generally, on-die termination (ODT) compensates for this, which may otherwise have a significant impact on signal quality and power dissipation.

Differential skew refers to the time difference between the two single-ended signals in a differential pair. Any mismatch in delay (skew) will result in changing part of the differential signal power into common-mode power.

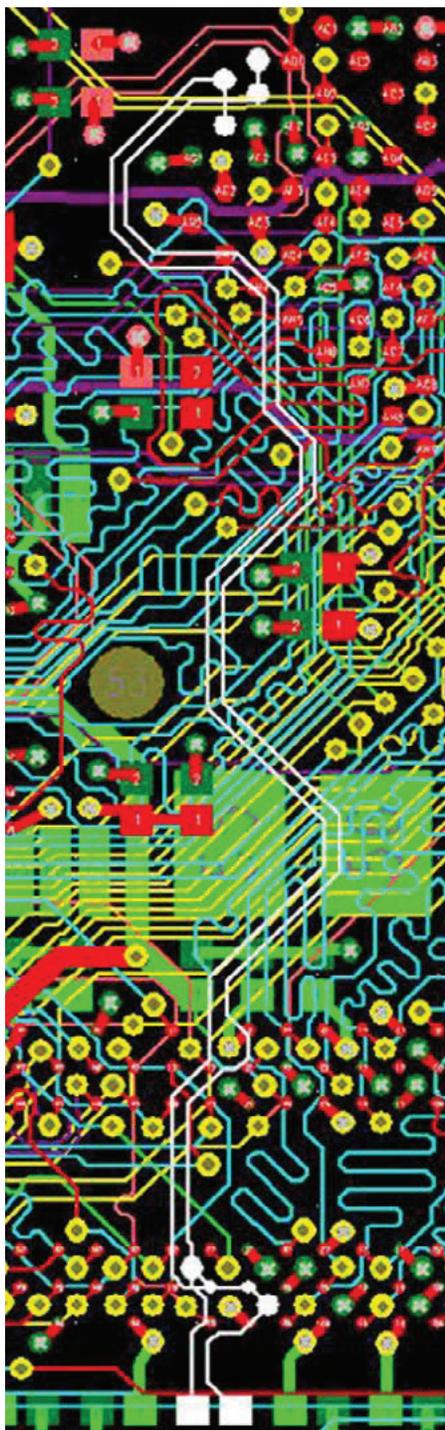


Figure 1: Multiple bends in the pair.

Differential skew has become a performance limiting issue for high-speed SERDES links. The operation of such links involves significant amounts of signal processing to recover clocks, reduce the effects of high-frequency losses, reduce inter symbol interference (ISI), and improve signal-to-noise ratio. Skew limits the bandwidth of these links, adds data-dependent jitter, and limits the possibility of equalizing links to compensate for high-frequency skin effect and dielectric losses.

Differential signaling evolved due to the fact that high-speed, synchronous, parallel busses were getting wider (consuming more real estate) and faster until signal integrity issues forced a fundamental change in strategy. Multi-gigabit design is now the norm with up to 10 Gbps SERDES devices commonly available in FPGAs. Beyond the theoretical 12 Gbps limit, optical interconnects become the only solution.

Skew is commonly caused by unmatched delays of a differential pair but as speeds (and rise times) increase skew can also be caused by non-uniform dielectric materials in the substrate.

The inconsistency of the dielectric material comes from that fact that the fiberglass and the epoxy resin that make

SKEWED AGAIN *continues*

up PCB core and prepreg materials have a different dielectric constant. And because the fabricator cannot guarantee the placement of the fiberglass with respect to the location of the traces, the result is uncontrolled differential skew. One way to avoid this is to always route differential pairs diagonally across the board as the fiberglass matting is laid in the X,Y direction. Or, zigzag diagonally down the board as done in Figure 1.

In, [Differential Pair Routing](#), (*The PCB Magazine*, October 2011) I discussed the optimal settings for differential pair design rules. With regard to coupling, I also pointed out that it is best to not use tight coupling but rather couple the traces by twice the trace width. Thus, for a differential pair with a trace width of 4 mils, the separation (edge-to-edge) should ideally be 8 mils. This allows the pair to separate (Figure 1) around an obstacle (e.g., a via) without altering the impedance by more than 4%.

However, wider spacing of the differential signals also means that the skew introduced by bends in the pair will increase. It is best to always have an even number of bends as one to the left will counteract one to the right.

Placement can also help alleviate this problem. Try to align the chips in such a way so that the traces leave the first chip (driver) and enter the second chip (receiver) from the same direction as this will result in an even number of

bends dramatically reducing skew.

Also, the squarer the bend, the more skew introduced. Arcs are shorter than 45 degree bends, which in turn are shorter than orthogonal corners. But if they are all the same then it does not matter.

In Figure 2, I have used orthogonal corners to illustrate the disparity between various routing strategies of differential pairs. The required number of bends depends on the number of obstacles that the pair encounters along its path. These obstacles may be other devices, lands, mounting holes or vias, which means that the traces may also have to be separated.

Pair A is obviously not the best example. This pair has two long bends on one side and two short bends on the other, adding a skew of twice the bend length to the outer trace. On the other hand, Pair B represents the best-case scenario whereby the pair leaves the driver in the same direction as they enter the receiver. This always provides an even number of short and long bends on both sides allowing the accumulated skew on both sides to be equal. Pair C, although it looks a lot worse than Pair A, actually has the same amount of skew as A. This pair leaves the driver to the right and then enters the receiver to the left requiring an odd number of short and long bends on each side of the pair.

A few months ago, I had the opportunity to analyze a design that had a number of high-

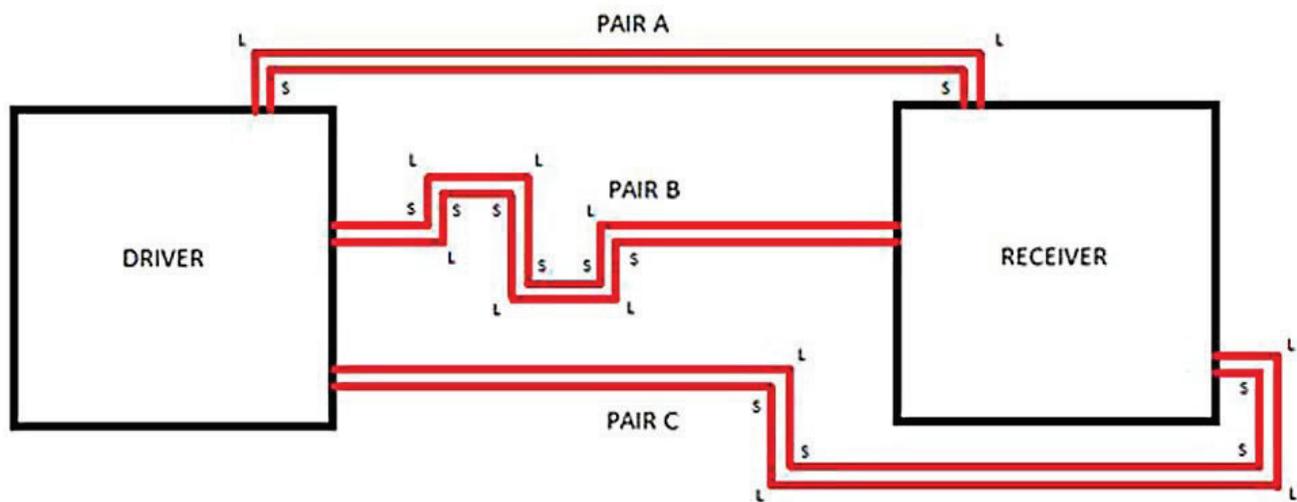


Figure 2: A driver and receiver chip with various routing strategies.

**SKEWED AGAIN** *continues*

speed USB 3.0 differential pairs. This was the first time I heard the term “cauliflower routing.” Cauliflower routing refers to a routing pattern as illustrated in Figure 3, whereby, one

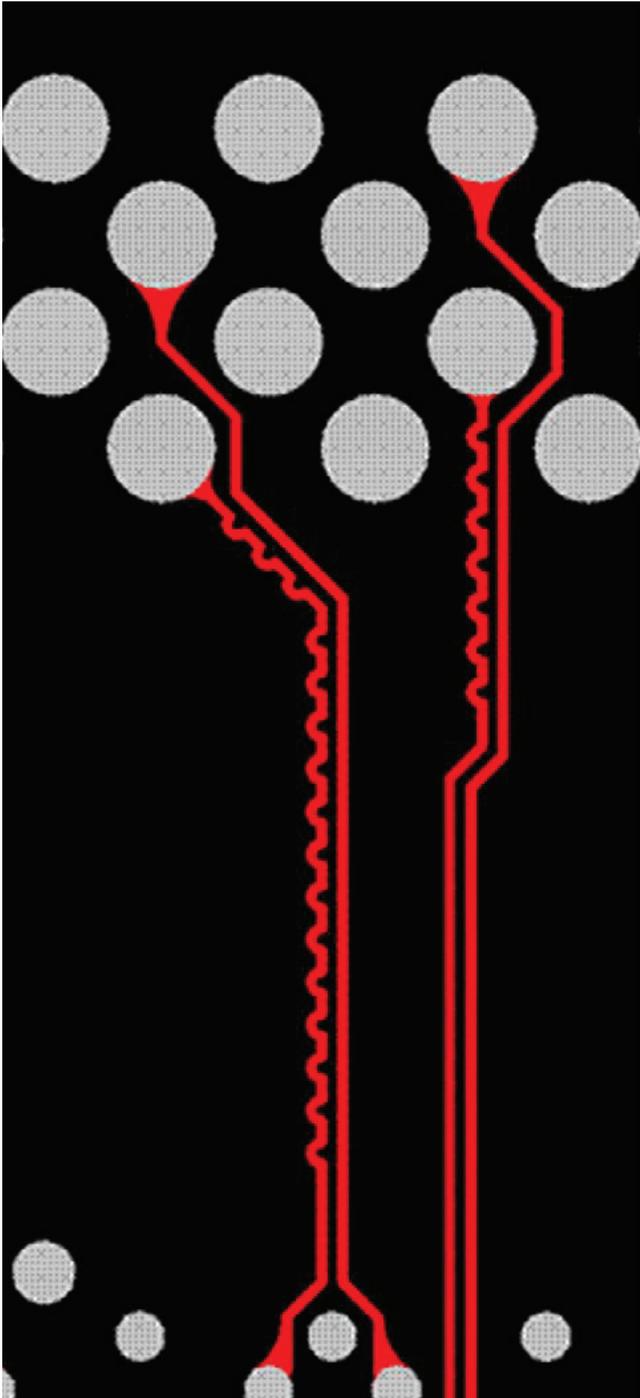


Figure 3: The dreaded cauliflower routing pattern.

side of the differential pair is lengthened by adding a number of semicircles (bumps). This is not good—please do not try this at home! The cauliflower pattern varied the differential impedance, in this example, from 90 ohms to 102 ohms. This dramatically reduces the quality of the signal adding numerous reflections.

In this case, the solution was simple. The USB 3.0 pairs went off the board through a connector to a piggy-back board that had the pins wired the opposite way around. This allowed the main board to be 200 mils longer for side A of the pair, and the piggy-back board side 200 mils longer for side B, thus cancelling out skew.

Since a differential pair is routed coupled, its entire length, the offset of one side of the pair to the other is rarely greater than 100 mils. So what is the best way to balance the skew?

When the skew needs to be adjusted, it is best done at either end of the pair—whichever has the poorest termination. In this way, the coupling and signal quality of the remainder of the pair is maintained along its length.

Figure 4 shows the skew control for coupled pairs. The idea is to keep the traces in close proximity for as long as possible. The trace to the left goes to pin AF3 on the BGA. To lengthen this side of the pair, we follow the other trace (on the right) as closely as possible and then wrap the left trace around the pin/land.

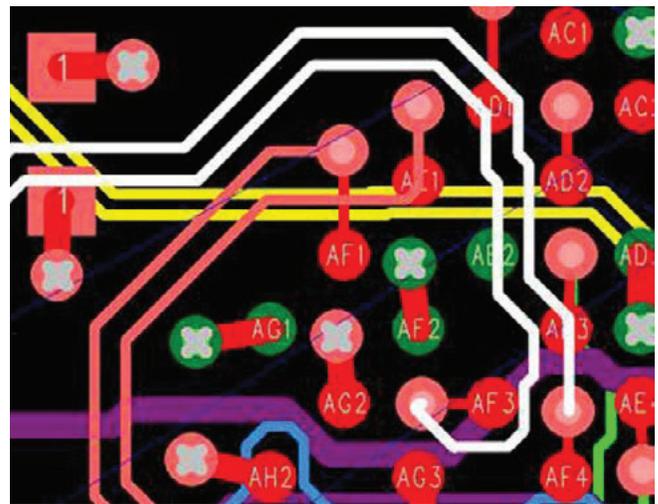


Figure 4: Skew matching is performed at the pin/land level.

Ideally, the delay of the differential pair should be confirmed by simulation rather than by matched length. I have mentioned in a couple of other columns on matched length and differential pair routing, that the length of the signal is not necessarily directly proportional to the delay. Delay can only be determined by simulation.

Points to remember:

- Any mismatch in delay (skew) will result in changing part of the differential signal power into common-mode power
- As speeds increase, skew can also be caused by non-uniform dielectric materials in the substrate
- It is best to not use tight coupling differential signals but rather couple the traces by twice the trace width
- It is good to always have an even number of bends as one to the left will counteract one to the right
- Align the chips in such a way so that the traces leave the first chip (driver) and enter the second chip (receiver) from the same direction. This always provides an even number of short and long bends, on both sides, allowing the accumulated skew on both sides to be equal
- Cauliflower routing should be avoided
- When the skew needs to be adjusted, this should be done at either end of the pair—whichever has the poorest termination. In this

way, the coupling and signal quality of the remainder of the pair is maintained

- Skew matching is performed at the pin/land level. The idea is to keep the traces in close proximity for as long as possible **PCBDESIGN**

### References

1. Advanced Design for SMT, Barry Olney
2. [Beyond Design: Differential Pair Routing](#), Barry Olney
3. [Beyond Design: A New Slant on Matched-Length Routing](#), Barry Olney
4. [Board Level Simulation and the Design Process: Plan B: Post Layout Simulation](#), Barry Olney
5. [Handling Differential Skew in High-Speed Serial Buses](#), Arnold Frisch
6. [High-Speed Signal Propagation](#), Howard Johnson
7. The ICD Stackup and PDN Planner can be downloaded from [www.icd.com.au](http://www.icd.com.au).



Barry Olney is managing director of In-Circuit Design Pty Ltd (ICD), Australia. ICD is a PCB design service bureau specializing in board-level simulation. The company developed the ICD Stackup Planner and ICD PDN Planner software. To read past columns or to contact Olney, [click here](#).

## IPC: Book-to-Bill Highest in Nearly Three Years

IPC has released the April 2013 PCB book-to-bill ratio, which reached 1.10, its highest level since July 2010.

North American PCB shipments were down 7% in April 2013 from April 2012, but bookings increased 7.2% YOY. Year to date, PCB industry shipments were down 5.1% and bookings were down 2.3%. Compared to March, PCB shipments in April decreased 9.9%, and bookings

declined 14.3%. Bookings have outpaced shipments for the past five months.

"This is the fifth consecutive monthly increase in the ratio, which reinforces our hope that PCB sales will strengthen during the coming months," said Sharon Starr, IPC director of market research.

