

# iCD Design Integrity

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**Dielectric Materials Library**  
30,700 Rigid & Flex Materials to 100GHz

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Extracts IV Curves from IBIS Models  
Calculates Series Terminator of the Distributed System Including Loads

**iCD Stackup Planner**  
Field Solver Accuracy, Characteristic Impedance, Edge & Broadside Coupled Impedance

**Extensive Capacitor Library**  
5,650 Decaps Derived from SPICE Models

**iCD PDN Planner**  
AC Impedance Analysis & Plane Resonance

**Matched Delay Optimization**  
Relative Signal Layer Propagation  
Ideal for DDRx Timing & Delay Modeling

**iCD Stackup Planner** - Offers Engineers & PCB Designers unprecedented simulation speed, ease of use and accuracy at an affordable price

- Industry Leading 2D (BEM) Field Solver precision
- Characteristic impedance, edge-coupled & broadside-coupled differential impedance
- Relative Signal Propagation with 'Matched Delay Optimization'—ideal for DDRx design
- Termination Planner - series termination based on IBIS models & distributed system
- Unique Field Solver computation of multiple differential technologies per signal layer
- Extensive Dielectric Materials Library—over 30,700 rigid & flexible materials up to 100GHz
- Interfaces—Allegro, Altium, Excel, HyperLynx, OrCAD, PADS, Zmetrix TDR, Zuken & IPC-2581B

**iCD PDN Planner** - Analyze multiple power supplies to maintain low AC impedance over entire frequency range dramatically improving product performance

- Fast AC impedance analysis with plane resonance and projected EMI
- Definition of plane size, dielectric constant & plane separation
- Extraction of plane data from the integrated iCD Stackup Planner
- Definition of voltage regulator, bypass/decoupling capacitors, mounting loop inductance
- PDN EMI Plot with FCC, CISPR & VCCI Limits. Frequency range up to 100GHz
- Extensive Capacitor Library—over 5,650 capacitors derived from SPICE models

*"iCD Design Integrity software features a myriad of functionality specifically developed for high-speed design."*  
- Barry Olney



# Plane Cavity Resonance

by Barry Olney

IN-CIRCUIT DESIGN PTY LTD / AUSTRALIA

Plane pairs in multilayer PCBs are essentially unterminated transmission lines—just not the usual traces or cables we may be accustomed to. They also provide a very low-impedance path, which means that they can present logic devices with a stable reference voltage at high frequencies. But as with signal traces, if the transmission line is mismatched or unterminated, there will be standing waves: ringing. The bigger the mismatch, the bigger the standing waves and the more the impedance will be location dependent.

Following on from my previous columns, [Return Path Discontinuities](#) and [The Dark Side—Return of the Signal](#), in this month's column, I will cover plane cavity resonance and look at how it impacts electromagnetic radiation.

When return current flows through the impedance of a cavity, between two planes, it generates voltage. Although quite small (typically in the order of 5mV) the accumulated noise from simultaneous switching devices can become significant. And unfortunately, as core voltages drop, noise margins become tighter. Figure 1, illustrates the electromagnetic fields resonating in a cavity. This voltage, emanating from the vicinity of the signal via, injects a propagating wave into the cavity which can excite the cavity resonances or any other parallel

structure (for instance, between copper pours over planes). Other signal vias also passing through this cavity can pick up this transient voltage as crosstalk.

The more switching signals that pass through the cavity, the more noise is induced into other signals; it affects vias all over the cavity, not just the ones in close proximity to the aggressor signal vias. This cavity noise propagates as standing waves spreading across the entire plane pair. This is the primary mechanism by which high frequency noise is injected into cavities—by signals transitioning through cavities, using each plane successively as the signal return path.

At low frequency, the cavity impedance (Figure 2) looks inductive due to the inductance of the voltage regulator module (VRM). However, the VRM inductance, combined with the plane resonance, produces an anti-resonance peak at ~35MHz, in this case. The plane resonance depends on a number of factors including conductor loss, plane area, dielectric constant and dielectric thickness between the plane pairs. In this example, the planes naturally resonate at ~300MHz with harmonics beginning at ~1GHz. If the AC impedance is high, at the fundamental frequency or at any of the odd harmonics, then the board will tend to radiate from the fringing fields at the edges of the planes.

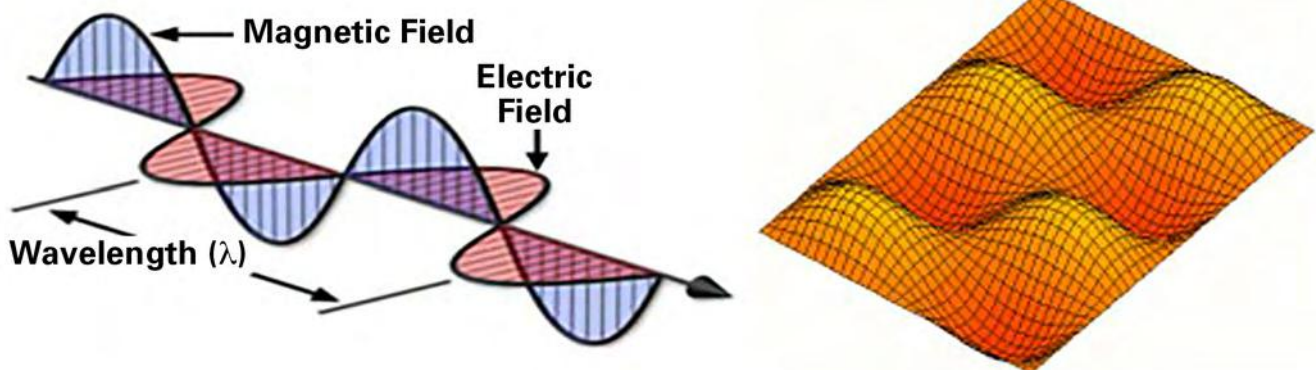


Figure 1: Electromagnetic fields propagating through a plane pair cavity (Source: Wikipedia).



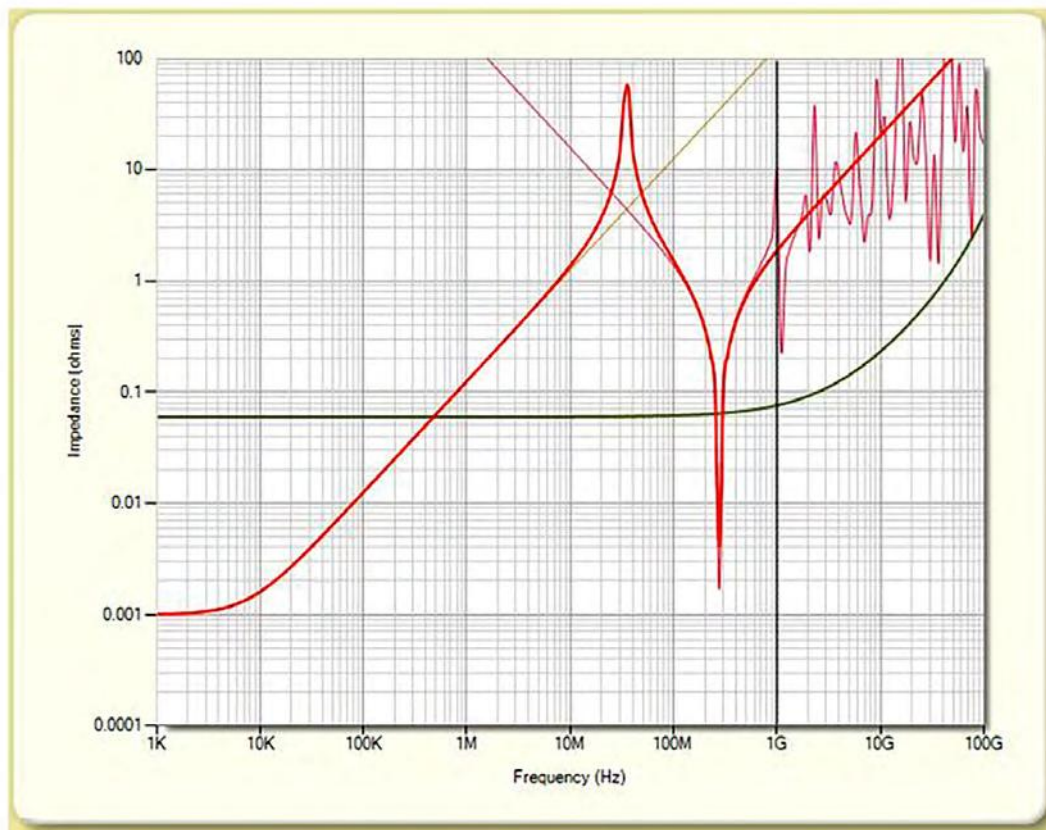


Figure 2: Impedance profile of a plane cavity with VRM (Source: iCD Design Integrity).

Signal paths are designed to be low Q resonators to dampen the ringing and to increase the bandwidth. However, cavities composed of a power and ground plane, can have very high Qs. This means even a slight amount of coupling, from signal paths, can drive resonances and give rise to long range noise voltages within the cavity. Knowing the cavity resonant frequencies, that one might encounter, can highlight potential problems.

When the cavity has open end boundary conditions, resonances arise when a multiple of half wavelengths can fit between the ends of the cavity. Figure 3 shows the cavity resonance of a plane pair with a resonant frequency of 1GHz. If the signal clock frequency (or harmonics) are multiples of 1GHz, then noise can be injected into the plane cavity. When the clock or data harmonics overlap with the cavity resonant frequencies, there is the potential for long range coupling between any signals that run through the cavity. This is one reason

why all return planes should be GND layers, so that stitching vias between GND planes can be placed adjacent to each signal via transition to minimize the possibility of exciting the cavity resonance.

Cavity resonances are (at first) a signal integrity issue but the amplification of cavity resonance excited by fast rise time signals, at high frequencies, can also contribute to electromagnetic emissions (EMI). The frequency components of the voltage noise are related to the peak impedance of the cavity and the frequency components of the return currents. In any complex system, with typical interconnect density, avoiding signal layer transitions is not practicable and is an issue that designers must live with. However, one can learn to avoid injecting excessive noise into the cavity or at least minimize the impact.

The goal of designing a high-performance cavity is to reduce the impedance peaks below the target impedance level and to push the peak

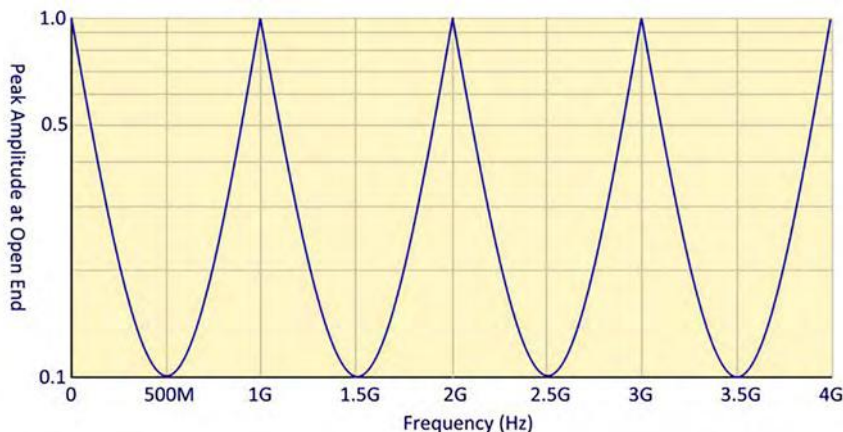


Figure 3: Amplitude at the far end of planes as input frequency is swept (Source: Eric Bogatin).

frequency components, above the bandwidth of the signals.

So, how should engineers and PCB designers go about reducing cavity resonance and emissions?

- A thin dielectric, in the plane cavity, is the most effective way of reducing the peak amplitude of the modal resonance. It reduces spreading inductance and the impedance, of the cavity, and also reduces the resonance peaks by damping the high-frequency components. Thinner plane separation implies less area of equivalent magnetic current at the plane pair edge, or equivalently less local fringing field volume, and therefore lower emissions for a given field strength.

- A dielectric material with a high dielectric constant (Dk) should be selected to add more planar capacitance. This is contrary to the typical choice of high-speed materials that require a low Dk. Remember; we are talking about the dielectric embedded between the planes, which has little impact of the signal properties.

- The parallel resonant frequencies, of the cavity, can be pushed up above the maximum bandwidth of the signals, by reducing the plane size and by adding stitching vias between (similar) planes of a cavity.

- Where the length of a rectangular plane is a simple multiple of its width, such as 1, 1.5 or 2, the resonant frequencies of the length and

width directions will coincide at some frequencies, causing higher-Q peaks—more intense resonances—than usual. So it is best to avoid square planes and simple L:W ratios by choosing irrational numbers.

- When plane pairs resonate, their emissions come from the fringing fields at the board edges. With ground/power plane pairs, edge-fired emissions can be reduced by reducing the plane separation, as described earlier, but this technique cannot generally be used for multiple planes. Alternatively, make the power planes slightly smaller

(~200 mil) than the GND plane. This modifies the pattern of the fringing fields, pulling them back from the edge, and may help reduce emissions to some extent.

Optimization of the PDN is a trial and error process. A combination of modifications to dielectric constant and thickness, of the material, together with an adjustment of plane size can usually establish the minimum resonance for a given configuration. Employing AC PDN analysis software (Figure 4) allows one to integrate the layer stack and dielectric materials with the PDN and enables visualization of these critical adjustments. If you can't see it, you can't fix it!

### Points to Remember

- Plane pairs, in multilayer PCBs, are essentially unterminated transmission lines.

- If a transmission line is mismatched or unterminated, there will be standing waves—ringing.

- When return current flows through the impedance of a cavity, between two planes, it generates voltage which can excite the cavity resonances.

- Other signal vias, also passing through this cavity, can pick-up this transient voltage as crosstalk.

- This cavity noise propagates as standing waves spreading across the entire plane pair.

- The slightest amount of coupling, from signal paths, can drive resonances and give rise to long range noise voltages within the cavity.

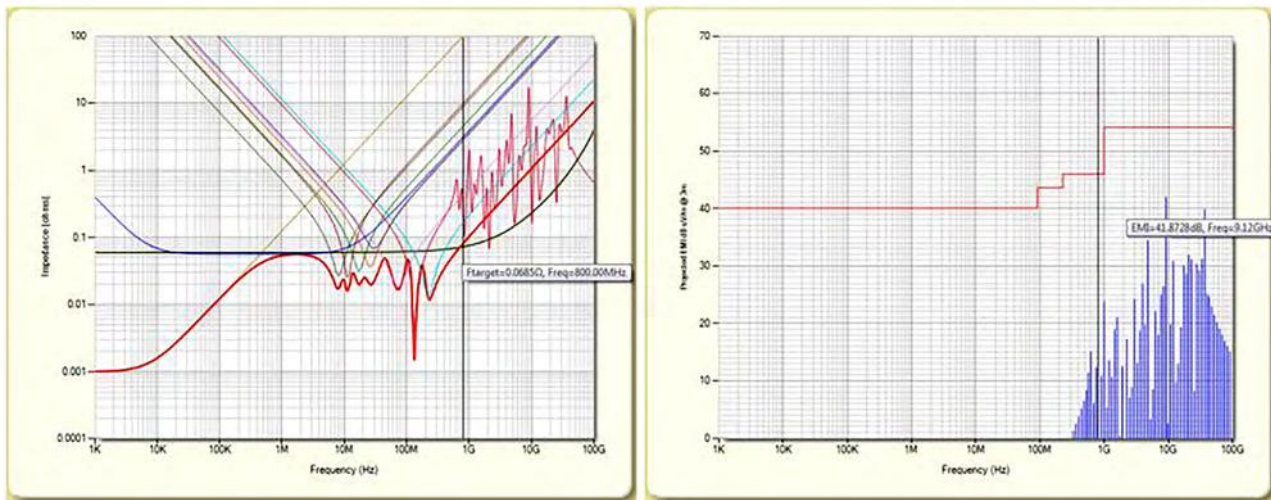


Figure 4: Optimized PDN with projected EMI (Source: iCD Design Integrity).

- When the cavity has open end boundary conditions, resonances arise when an integral multiple of half wavelengths can fit between the ends of the cavity.

- When the clock or data harmonics overlap with the cavity resonant frequencies, there is the potential for long range coupling between any signals that run through the cavity.

- Stitching vias between GND planes can be placed adjacent to each signal via transition to minimize the possibility of exciting the cavity resonance.

- The frequency components of the voltage noise are related to the peak impedance of the cavity and the frequency components of the return currents.

- The goal of designing a high-performance cavity is to push the peak frequency components, above the bandwidth of the signals, and to reduce the impedance peaks below the target impedance level.

- A thin dielectric, in the plane cavity, is the most effective way of reducing the peak amplitude of the modal resonance.

- A dielectric material with a high dielectric constant (Dk) should be selected to add more planar capacitance.

- Effective ways of pushing up the parallel resonant frequencies is by reducing the plane size and by adding stitching vias between (similar) planes of a cavity.

- Avoid square planes and simple L:W ratios by choosing irrational numbers.

- Make the power planes slightly smaller than the GND plane. This modifies the shape of the fringing fields, pulling them back from the edge. **PCBDESIGN**

### References

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5. [High-Speed Digital Design](#), by Howard Johnson



**Barry Olney** is managing director of In-Circuit Design Pty Ltd (iCD), Australia, a PCB design service bureau that specializes in board-level simulation. The company developed the iCD Design Integrity software incorporating the iCD Stack-up, PDN and CPW Planner. The software can be downloaded from [www.icd.com.au](http://www.icd.com.au). To contact Olney, or read past columns, [click here](#).