The Perfect Stackup (for high speed design)

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This application note discusses how to plan a multilayer PCB stackup to obtain the ideal stackup for high speed design

Over the past 30 years the concept of the perfect stackup has changed considerably. Especially in more recent years, where Engineers and Designers have had the opportunity to use simulation tools that act as another pair of eyes when it comes to understanding the intricacies of the effects of transmission lines on multilayer PCB's.

In previous articles, I have discussed the selection of reference planes and routing pairs, why high speed signals should be embedded between the planes and methods of reducing EMI. But, if we fail to get the substrate correct then all of the above techniques are worthless. Planning the multilayer stackup configuration is one of the most important aspects in achieving the best possible performance of a product yet it is something that few of us do (or should I say do well).

A poorly designed substrate, with inappropriately selected materials, can degrade the electrical performance of signal transmission increasing emissions and crosstalk and can also make the product more susceptible to external noise. These issues can cause intermittent operation due to timing glitches and interference dramatically reducing the products performance and long term reliability.

In contrast, a properly built PCB substrate can effectively reduce electromagnetic emissions, crosstalk and improve the signal integrity providing a low inductance Power Distribution Network (PDN). And, looking from a fabrication point of view, can also improve the manufacturability of the product and reduce costs.

Suppressing the noise at the source rather than trying to elevate the problems once the product has been built makes sense. Having the project completed 'Right First Time' on time and to budget means that you cut costs by reducing the design cycle, have a shorter time to market and an extended product life cycle.

Interplane Capacitance

A good place to start is with the PDN. Or more importantly, how we can provide a low inductance PDN and thus reduce the high frequency noise.

Decoupling capacitors (Dcap's) supply instantaneous current (at different frequencies) to the drivers until the power supply can respond. In other words, it takes a finite time for current to flow from the power supply circuit (whether on-board or remote) due to the inductance of the trace and/or leads to the drivers.

Every decoupling capacitor has a finite series inductance which causes it's impedance to increase at high frequencies. In order to reduce this inductance, as much as possible, a number of small value Dcap's should be placed in parallel as close as possible to each power pin using a thick short trace. This is not always possible as circuit density increases with the use of fine pitch BGA's so an alternative option is to take advantage of interplane capacitance to distribute capacitance across the board. This is not to say that the Dcap's aren't required – every little bit counts.

The power to ground plane capacitance provides an ideal capacitor in that it has no series lead inductance and no equivalent series resistance (ESR), which helps reduce noise at extremely high frequencies.

The interplane capacitance needs to be calculated to establish the optimal use of the planes to create the ideal stackup.

$$C\ interplane = \frac{0.225.Er.A}{d}$$

where: Er is the Dielectric Constant (FR4 is 4.3)
A is the area of the PCB
d is the distance between the planes

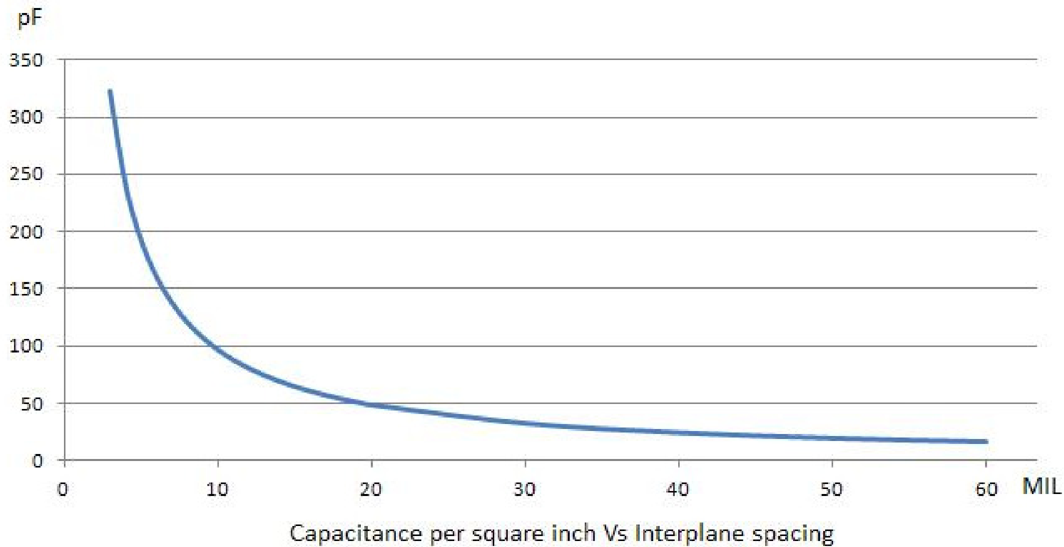

Fig. 1

Good interplane capacitance can be achieved by using 4 MIL plane spacing resulting in 241 pF/in^2. The higher the better. Whereas, 10 MIL spacing will only achieve 96.75 pF/in^2 and 60 MIL a dismal 16 pF/in^2. So this goes right in the middle of the substrate to maintain symmetry.

Layer		Material	Dielectric		Copper	Trace		Current	Impedance	Edge Coupled	Broadside Coupled	
Number	Name	Type	Constant	Thickness	Thickness	Clearance	Width	(Amps)	Characteristic(Zo)	Differential(Zdiff)	Differential(Zdbs)	Description
1	VCC	Conductive			1.4							Plane
		Dielectric	4.3	4								Core
2	GND	Conductive			1.4							Plane

Fig. 2 Interplane capacitance is 241 pF/in^2

Reference Planes and Signal Layers

The next step, in building the ideal stackup, is to consider that every signal layer needs to have a reference plane (either ground or power) adjacent to it in order to provide a return current path. This limits the number of signal layers embedded between the planes to two and on the top and bottom (outer) layers to one.

However, routing two signals layers between planes is not a good idea for high speed designs as the close proximity of signals will inevitably create broadside coupling (crosstalk) unless the two signal layers are routed orthogonally to each other to limit the coupling area. So this limits the stackup to one signal layer between planes.

Layer		Material	Dielectric		Copper	Trace		Current	Impedance	Edge Coupled	Broadside Coupled	
Number	Name	Type	Constant	Thickness	Thickness	Clearance	Width	(Amps)	Characteristic(Zo)	Differential(Zdiff)	Differential(Zdbs)	Description
2	GND	Conductive			1.4							Plane
		Dielectric	4.3	8								Core
3	Inner 3	Conductive			1.4	8	4	0.31	62.39	99.59		Signal
		Dielectric	4.3	12								Prepreg
4	VCC	Conductive			1.4							Plane
		Dielectric	4.3	4								Core
5	GND	Conductive			1.4							Plane

Fig. 3 Inner layer 3, 100 ohm differential pairs

Inner layer 3 is added in Fig. 3. This will provide 100 ohm differential clocks at 4/8 (trace width/clearance). Or, in Fig. 4 we change the trace width/clearance to 7/16, using the same substrate, to provide USB differential signals of 90 and 50 ohm single ended (characteristic) impedance on this layer.

Layer		Material	Dielectric		Copper	Trace		Current	Impedance	Edge Coupled	Broadside Coupled	
Number	Name	Type	Constant	Thickness	Thickness	Clearance	Width	(Amps)	Characteristic(Zo)	Differential(Zdiff)	Differential(Zdbs)	Description
2	GND	Conductive			1.4							Plane
		Dielectric	4.3	8								Core
3	Inner 3	Conductive			1.4	16	7	0.47	50.72	89.54		Signal
		Dielectric	4.3	12								Prepreg
4	VCC	Conductive			1.4							Plane
		Dielectric	4.3	4								Core
5	GND	Conductive			1.4							Plane

Fig. 4 USB differential pairs of 90 ohm

Soldermask – Affects on Impedance

Another point that is often missed is the affects of soldermask (conformal coating) on microstrip (outer layer) impedance. Without soldermask the differential impedance of the top microstrip layer is 103.94 ohm.

Layer		Material	Dielectric		Copper	Trace		Current	Impedance	Edge Coupled	Broadside Coupled	
Number	Name	Type	Constant	Thickness	Thickness	Clearance	Width	(Amps)	Characteristic(Zo)	Differential(Zdiff)	Differential(Zdbs)	Description
1	Top	Conductive			1.4	8	4	0.31	55.64	103.94		Signal
		Dielectric	4.3	3								Prepreg
2	GND	Conductive			1.4							Plane
		Dielectric	4.3	8								Core
3	Inner 3	Conductive			1.4	8	4	0.31	62.39	99.59		Signal
		Dielectric	4.3	12								Prepreg
4	VCC	Conductive			1.4							Plane
		Dielectric	4.3	4								Core
5	GND	Conductive			1.4							Plane

Fig. 5 Microstrip layer without soldermask

Adding the soldermask to Fig. 6 illustrates how the impedance drops by nearly 4 ohms for the differential pair and 2 ohms for the signal ended trace. So if you don't consider soldermask then the calculation could be as much as 4% out, which is significant since the process margin is +/- 10%.

Layer		Material	Dielectric		Copper	Trace		Current	Impedance	Edge Coupled	Broadside Coupled	
Number	Name	Type	Constant	Thickness	Thickness	Clearance	Width	(Amps)	Characteristic(Zo)	Differential(Zdiff)	Differential(Zdbs)	Description
		Dielectric	3.3	0.5								Soldermask
1	Top	Conductive			1.4	8	4	0.31	53.53	99.99		Signal
		Dielectric	4.3	3								Prepreg
2	GND	Conductive			1.4							Plane
		Dielectric	4.3	8								Core
3	Inner 3	Conductive			1.4	8	4	0.31	62.39	99.59		Signal
		Dielectric	4.3	12								Prepreg
4	VCC	Conductive			1.4							Plane
		Dielectric	4.3	4								Core
5	GND	Conductive			1.4							Plane

Fig. 6 Soldermask over microstrip

It is also important to note that particularly on the outer microstrip layers the signal to plane spacing should be kept to a minimum. This reduces crosstalk significantly.

Having determined the basic structure of the stackup with the aid of the ICD Stackup Planner (download from www.icd.com.au) we now need to consider how many layers will be required to route the board.

Determining the Layer Count

The technology rules are based on the minimum pitch of the SMT components employed and are basically the largest trace, clearance and via allowable whilst minimizing PCB fabrication costs. Technology of 4/4 MIL (trace/clearance) and Vias of 20/8 MIL (pad/hole) are generally required for complex high speed design incorporating ball grid arrays (BGA). However, if you can use less demanding dimensions then this will reduce cost and improved fabrication yield.

Once these rules have been established, calculate the stackup required for the desired characteristic impedance (Zo) and the differential impedance (Zdiff) as per the component datasheets. Generally, 50 ohm Zo and 100 ohm Zdiff are used. Keep in mind that lower impedance will increase the dI/dt and dramatically increase the current drawn (not good for the PDN) and higher impedance will emit more EMI and also make the design more susceptible to outside interference. So, a good range of Zo is 50 – 60 ohms.

The total number of layers required for a given design is dependent on the complexity of the design. Factors include: the number of signal nets that must break out from a BGA; the number of power supplies required by the BGA's; component density and package types.

Experienced Designers get a feel for it after a while but a good way to check if you have enough layers is to autoroute the board. With no tweaking, the autorouter needs to complete at least 85% of the routes to indicate the selected stackup is routable. The performance of the autorouter also impacts on the completion rate. You may have to re-evaluate the placement a couple of times to get the best results.

UNITS: MIL | ICD STACKUP PLANNER – www.icd.com.au | 9/27/2011 | Total Board Thickness: 61.2

Differential Pairs > USB | DDR2 | SATA | ETHERNET | LVDS

Layer		Material	Dielectric		Copper	Trace		Current	Impedance	Edge Coupled	Broadside Coupled	
Number	Name	Type	Constant	Thickness	Thickness	Clearance	Width	(Amps)	Characteristic(Zo)	Differential(Zdiff)	Differential(Zdbs)	Description
		Dielectric	3.3	0.5								Soldermask
1	Top	Conductive			1.4	8	4	0.31	53.53	99.99		Signal
		Dielectric	4.3	3								Prepreg
2	GND	Conductive			1.4							Plane
		Dielectric	4.3	8								Core
3	Inner 3	Conductive			1.4	8	4	0.31	62.39	99.59		Signal
		Dielectric	4.3	12								Prepreg
4	VCC	Conductive			1.4							Plane
		Dielectric	4.3	4								Core
5	GND	Conductive			1.4							Plane
		Dielectric	4.3	12								Prepreg
6	Inner 6	Conductive			1.4	12	6	0.42	54.11	91.56		Signal
		Dielectric	4.3	8								Core
7	GND	Conductive			1.4							Plane
		Dielectric	4.3	3								Prepreg
8	Bottom	Conductive			1.4	4	4	0.31	53.53	89.98		Signal
		Dielectric	3.3	0.5								Soldermask

Fig. 7 Completed eight layer stackup

The above stackup represents the perfect stackup. Why perfect?

- There is good interplane capacitance of 241 pF/in ^{2}.
- All signal layers are adjacent to a reference plane creating a clear return path and eliminating broadside crosstalk.
- The signal ended and differential impedance for a number of different technologies that must share the sample layers is determined.
- Microstrip layers are closely coupled to the planes reducing crosstalk.
- The affects of soldermask on impedance have been realized.

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UNITS: MIL ICD STACKUP PLANNER – www.icd.com.au 9/27/2011 Total Board Thickness: 90.8

Differential Pairs > USB DDR2 SATA ETHERNET LVDS

Layer		Material	Dielectric		Copper	Trace		Current	Impedance	Edge Coupled	Broadside Coupled	
Number	Name	Type	Constant	Thickness	Thickness	Clearance	Width	(Amps)	Characteristic(Zo)	Differential(Zdiff)	Differential(Zdbs)	Description
		Dielectric	3.3	0.5								Soldermask
1	Top	Conductive			1.4	8	4	0.31	53.53	99.99		Signal
		Dielectric	4.3	3								Prepreg
2	GND	Conductive			1.4							Plane
		Dielectric	4.3	6								Core
3	Inner 3	Conductive			1.4	12	4	0.31	56.4	98.4		Signal
		Dielectric	4.3	10								Prepreg
4	GND	Conductive			1.4							Plane
		Dielectric	4.3	6								Core
5	Inner 5	Conductive			1.4	12	4	0.31	56.4	98.4		Signal
		Dielectric	4.3	10								Prepreg
6	VCC	Conductive			1.4							Plane
		Dielectric	4.3	4								Core
7	GND	Conductive			1.4							Plane
		Dielectric	4.3	10								Prepreg
8	Inner 8	Conductive			1.4	12	5	0.37	51.96	90.66		Signal
		Dielectric	4.3	6								Core
9	VDD	Conductive			1.4							Plane
		Dielectric	4.3	10								Core
10	Inner 10	Conductive			1.4	6	4	0.31	56.4	89.06		Signal
		Dielectric	4.3	6								Prepreg
11	GND	Conductive			1.4							Plane
		Dielectric	4.3	3								Prepreg
12	Bottom	Conductive			1.4	4	4	0.31	53.53	89.98		Signal
		Dielectric	3.3	0.5								Soldermask

Fig. 8 12 layer extension of the ideal eight layer PCB

So if you are risk aversive – then this is the stackup to use. This can of course be extrapolated to include more routing layers if there is a need. Simply keep the closely coupled planes in the centre and add more signals layers and planes keeping symmetry. The dielectric thickness' may also need to be adjusted to achieve the desired impedances and total board thickness. The selection process can be simplified by using the HDI Designer Edition of the ICD Stackup Planner which assists in the definition of multiple technologies sharing the one substrate and allows groups of layers to be cut/copied/pasted to build up a substrate. I have provided an example of adding two more routing layers in the 12 layer stackup of Fig. 8.

References

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Right First Time Design – Lee Ritchie
EMC Compatibility Engineering – Henry Ott Consultants
ICD Stackup Planner – In-Circuit Design Pty Ltd (available for download @ www.icd.com.au)

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