

BOARD LEVEL SIMULATION SPECIALISTS

ICD Stackup Planner - offers engineers/PCB designers unprecedented simulation speed, ease of use and accuracy at an affordable price

- 2D (BEM) field solver precision
- Characteristic impedance, edge-coupled & broadside-coupled differential impedance
- Unique field solver computation of multiple differential technologies per stackup
- Heads-up impedance plots of signal and dielectric layers
- User defined dielectric materials library - over 16,250 materials up to 100GHz

ICD PDN Planner - analyze multiple power supplies to maintain low impedance over entire frequency range dramatically improving product performance

- Fast AC impedance analysis with plane resonance
- Definition of plane size/shape, dielectric constant & plane separation for each on-board power supply
- Extraction of plane data from the integrated Stackup Planner
- Definition of voltage regulator, bypass/decoupling capacitors, mounting loop inductance
- Frequency range up to 100GHz
- Extensive Capacitor Library – over 5,250 capacitors derived from SPICE models

PDN Planning and Capacitor Selection, Part 1

by Barry Olney

IN-CIRCUIT DESIGN PTY LTD | AUSTRALIA

In my first column on power distribution network (PDN) planning, [Beyond Design: Power Distribution Network Planning](#), I described the basics of planning for low AC impedance between the planes, in order to reduce supply noise and provide reliable performance. I recommend that you read that column first to get the required background knowledge.

This column will focus on capacitor selection and three alternative approaches to analyzing the PDN:

1. Target frequency
2. One value capacitor per decade
3. Optimized value capacitor

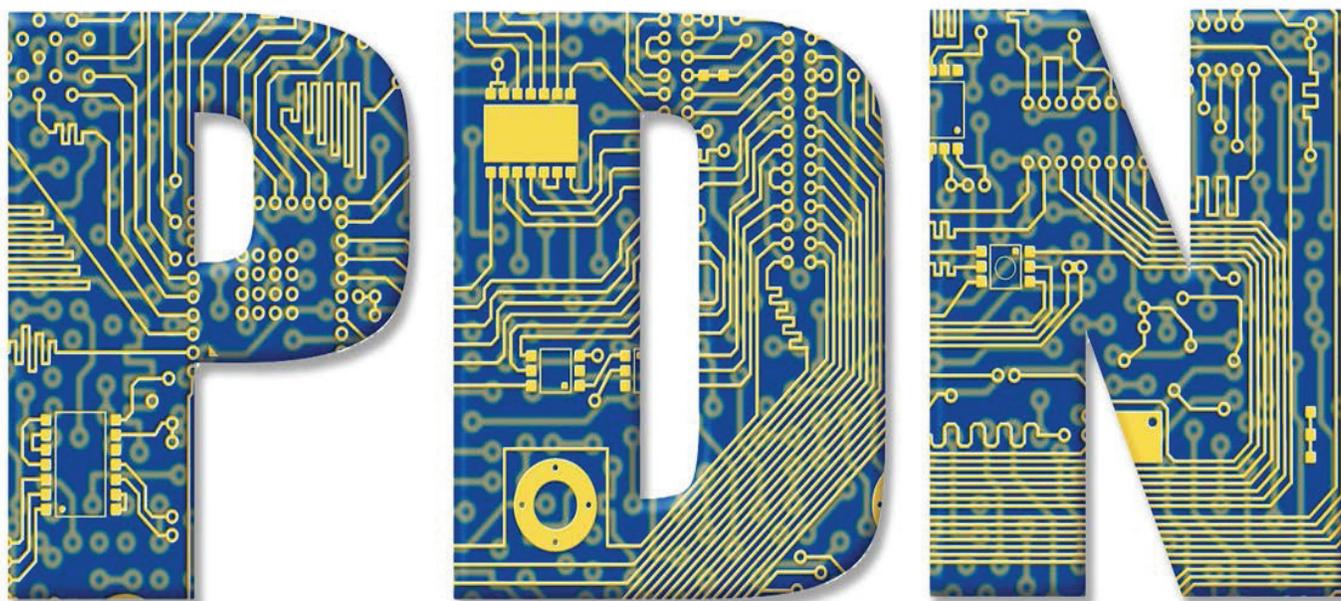
Traditionally, the target frequency approach has been used. This method targets a precise frequency and is used to reduce AC impedance and can also be used to reduce EMI within a specific band. The alternatives of using either one value capacitor per decade or many opti-

mized capacitors, is an attempt to level out the AC impedance, at the desired impedance, over a broad frequency band.

The latest high-performance processors, with sub-nanosecond switching times, use low DC voltages with high transient currents and high clock frequencies to minimize the power consumption and hence, heat dissipated. Fast rise times, low output buffer impedance and the simultaneous switching of busses create high transient currents in the power and ground planes degrading performance and reliability of the product.

Poor PDN design can result in unusual, intermittent signal integrity issues including high crosstalk and excessive emission of radiation. It can be extremely difficult to track down the cause of such issues, so my recommendation is to plan the PDN design prior to place and route in a pre-layout analysis of the design.

The integrity of the PCB stackup and the PDN are the basis for a stable product. Multi-



PDN PLANNING AND CAPACITOR SELECTION, PART 1 *continues*

layer PCB design is becoming more complex and less forgiving—it's not just about signal integrity, crosstalk and EMI. The substrate and the power delivery system are extremely critical and if they should fail then the whole system can go down or worse case, may just work intermittently.

Choosing the Right Capacitors

Many application notes say all we need to do is add three capacitors per power pin. Some recommend using three different values; others say they should all be the same value. But which is right, or are they both wrong? Decoupling is not the process of placing a capacitor adjacent to the IC power pin, but rather it is the process of placing an L-C network adjacent to the IC to supply the high transient switching current. The inductance comes from the capacitor itself, the lands, the interconnecting traces and vias and the lead frame of the IC—collectively—the loop inductance. It is this inductance that limits the effectiveness of the decoupling network.

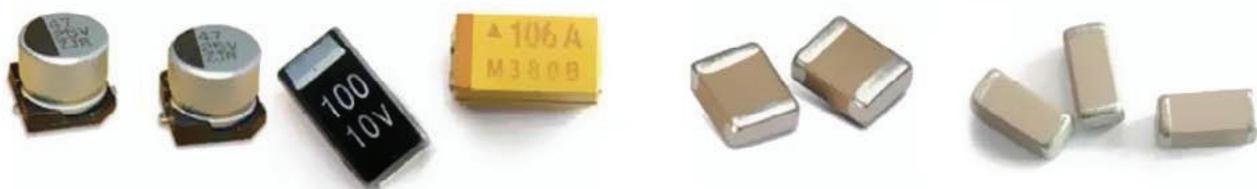
Decoupling capacitors supply instantaneous current, at different frequencies, to the drivers until the power supply can respond. In other words, it takes a finite time for current to flow from the power supply circuit, whether on-board or remote, due to the inductance of the traces and/or leads to the drivers. Each capacitor added to the board lowers the impedance of the PDN at a particular frequency. Bulk bypass capacitance—typically provided by tantalum capacitors—provide low impedance up to 10MHz. High-frequency decoupling is provid-

ed by ceramic capacitors up to several 100MHz. Above 200MHz, high-quality, low-inductance capacitance is necessary to support the very fast switching transients associated with driving single ended transmission lines and rapidly-changing IC core-supply currents. This is provided by the on-die capacitors or capacitance formed by adjacent power and ground layers.

For bulk decoupling at the supply level, tantalum is usually preferred, due to the availability of high capacitance ratings. At the IC level, and sometimes at the power supply, ceramic may be preferred due to its low equivalent series resistance (ESR) and excellent high frequency response. Design characteristics of the ceramic also allow low-inductance designs that reduce noise generated at the initial di/dt energy transfers.

Large capacitance value ceramics provide effective decoupling at about 25% of the nominal capacitance value compared to standard tantalums. This is because the capacitance of the ceramic is more stable with increasing frequency, while that of the tantalum and aluminum electrolytics tend to roll off, making them respond as much smaller capacitance values than the nominal rating. In addition, the lower ESR of the ceramics reduces the total capacitance required to maintain the desired voltage. Ceramics range in capacitance from 12pF to ~10uF.

New types of polymer tantalum and aluminum capacitors also have better capacitance stability and lower ESR than do older types, which permit the user to substitute lower nominal capacitance values in the circuits. There are



Tantalum

Capacitance (high)	0.1uF – 680uF
SRF (low)	127KHz – 12MHz
Voltage (low)	3V – 50V

Ceramic

Capacitance (low)	0.75pF – 100uF
SRF (high)	490KHz – 8.3GHz
Voltage (high)	5V – 200V

Figure 1: Examples of tantalum and ceramic capacitors.

Material	Dielectric Constant	% Capacitance Change	Df %
NPO	15–100	< 0.4	0.1
X7R	2,000–4,000	+/- 15	3.5
Y5V	> 16,000	< 82	9

Table 1: Critical specifications of MLCCs.

also applications where the bulk capacitance requirements are so high that the volumetric efficiency of the tantalum makes it the preferred type.

Over the years, capacitor sizes have shrunk dramatically. Multilayer ceramic capacitors (MLCCs) are the most commonly used decoupling capacitors for high-speed design as they are small and have relatively high capacitance values for their size. MLCCs are produced from alternating layers of ceramic and metal to produce a multilayer capacitor.

The capacitance value of a capacitor is determined by three factors: the number of layers in the part, the dielectric constant, and the active area. The dielectric constant is determined by the ceramic material (NPO, X7R, X5R, or Y5V). The active area is the overlap between two opposing electrodes.

The dielectric thickness is inversely related to the capacitance value, so the thicker the dielectric, the lower the capacitance value. This also determines the voltage rating of the part, with the thicker dielectric having a higher volt-

age rating than the thinner one. This is why the basic trade-off in MLCCs is between voltage and capacitance.

The rating compared to working voltage for MLCCs is 2:1. This means that, for a rail voltage of 1.8V as used for DDR2, the voltage rating needs to be 3.6V. So a standard 6.3V capacitor can be used with most processors.

The dielectric constant depends on the ceramic material used. Table 1 shows different dielectrics and some of their specifications. As you can see, NPO has the lowest dielectric constant, followed by X7R which has a significantly higher constant, and Y5V which is higher still. This is why the capacitance values for X7R capacitors are much higher than NPO capacitors, and Y5V has higher capacitance than X7R. The capacitance change vs. temperature is very small for NPO parts from -55°C–125°C, and gets larger for X7R, then even larger for Y5V. So the more capacitance a material provides, the lower the stability of capacitance over temperature.

Dissipation factor (Df) is the percentage of energy radiated as heat in the capacitor. As you

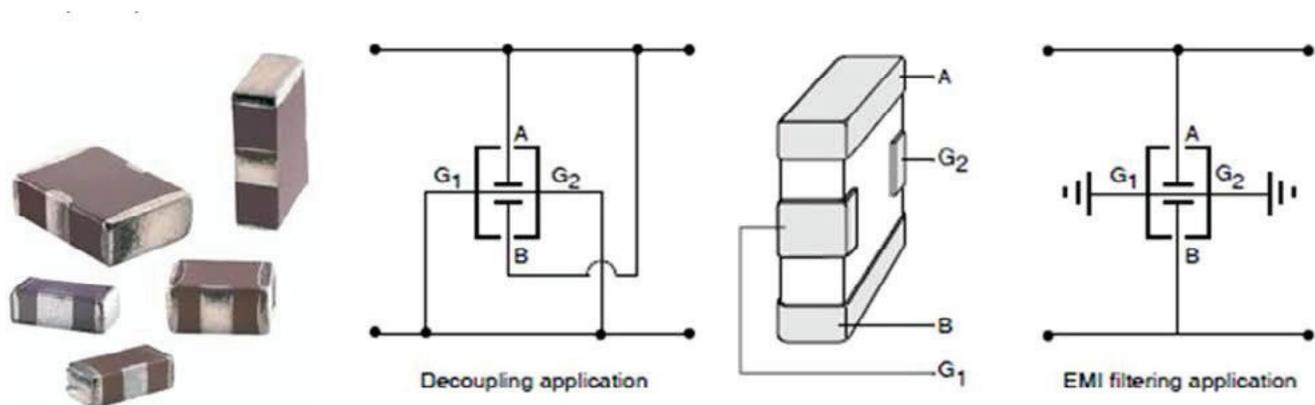


Figure 2: X2Y capacitor and equivalent circuit. (courtesy Yageo)

PDN PLANNING AND CAPACITOR SELECTION, PART 1 *continues*

can see, NP0 material is very efficient, followed by X7R, then Y5V which is the least efficient of the three materials.

The capacitance of all ceramic capacitors changes with temperature, voltage, frequency and over time. COG (aka NP0) capacitors are very stable and are manufactured in sizes up to 10nF, while X7R capacitors are less stable, and manufactured in sizes up to 1uF. A third common type is Z5U, which is of very low grade, and not recommended.

Another type of MLCC is the X2Y series. They are comprised of two identical Y-capacitors and one X-capacitor, integrated into a four-terminal device, and are available in standard MLCC sizes (0603, 0805, 1206, etc.).

X2Y filter capacitors employ a low inductance design featuring two balanced capacitors that are immune to temperature, voltage and aging performance differences. These components offer superior decoupling and EMI filtering performance and virtually eliminate parasitics. When used in EMI filtering configuration, the X2Y capacitor is connected across two signal lines. Differential-mode noise is filtered to ground by the two Y capacitors, A and B. Common-mode noise is cancelled within the device. A and B capacitors are placed in parallel, in the decoupling application, effectively doubling the capacitance while maintaining an ultra-low inductance. While X2Y MLCCs offer superior performance and are better space-wise (four X2Ys are equivalent in size to six 0402s), they are about five times the price of a standard 0402.

Tantalum capacitors that lower the impedance at the low-frequency end of the scale are less critical. Tantalums come in larger packages, from the 0805 and 1206 region to 2917, and they range from 0.1 to 680uF. Obviously, it is best to choose a low ESR and low equivalent series inductance (ESL) for the same capacitance value.

A capacitor's equivalent circuit is basically a series capacitor,

resistor and inductor. These are referred to as the capacitance value, ESR and ESL respectively. Generally, the ESR and ESL are not listed in data-sheets but rather are extracted by a SPICE simulator. This is because the ESL of the capacitor is rather meaningless as the bulk of the inductance is attributed to the loop inductance due to mounting the capacitor. The capacitor's self-resonant frequency (SRF) can be calculated by:

$$SRF = \frac{1}{2\pi\sqrt{LC}}$$

Looking at Figure 3, we can see that the downward slope of the capacitor is capacitive, then as the capacitor approaches its SRF it becomes resistive and as the frequency increases the inductance takes over raising the impedance again. So basically, the capacitor only has low impedance for a very small bandwidth about the resonant frequency—and high either side of this frequency band. But the goal of PDN planning is to make the AC impedance, of the entire PDN, look like a resistor, flat from zero to infinity, but in reality this does not happen.

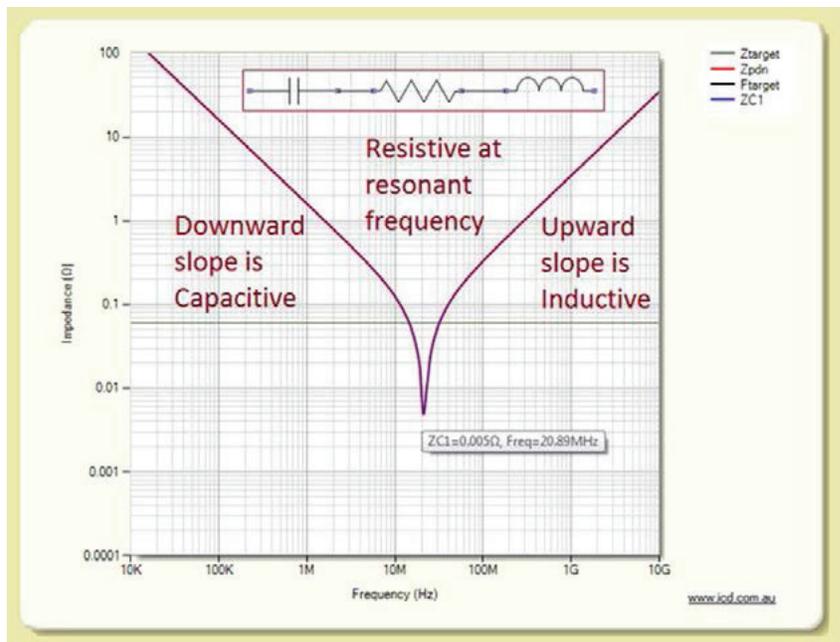


Figure 3: A capacitor has series capacitance, resistance and inductance.

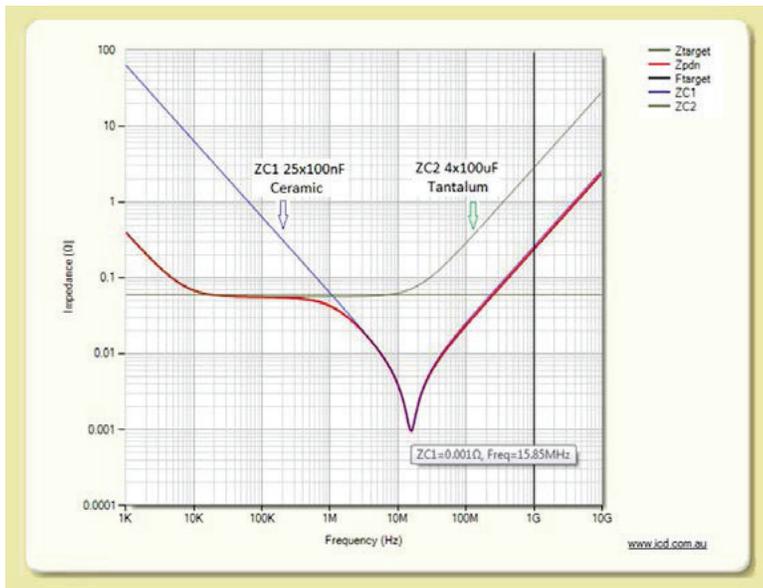
PDN PLANNING AND CAPACITOR SELECTION, PART 1 *continues*

Figure 4: The target frequency approach.

To meet the target (low) impedance at a particular frequency, a capacitance value is chosen so that when mounted on the PCB, it will resonate at the desired frequency, and have an impedance that is equal to its ESR. Then a sufficient number of those capacitors are placed in parallel so that the parallel ESRs approach the desired target impedance.

When N equal L-C networks are placed in parallel:

$$\text{Total capacitance} = N \times C \quad | \quad \text{Total Inductance} = L/N$$

$$Z = \sqrt{\frac{L}{C}}$$

Both work in our favor, and for a fixed PDN inductance, the effectiveness is solely dependent on the number of capacitors (N).

- The more capacitors (N) the lower the total inductance, and the better the high-frequency decoupling
 - Typical “ N ” values range from 4–25 decaps, though it varies by application
 - When a large number of capacitors are used, their placement becomes less critical than

when only 1-2 caps are used—spread them out around the IC, and try to place them symmetrically (and evenly) with respect to the IC

In Figure 4, the ICD PDN planner, available from www.icd.com.au, illustrates 25 x 100nF 0402 ceramic and 4 x 100uF 1210 tantalum capacitors in parallel to achieve the desired target impedance from 20KHz to 250MHz for a particular PDN. But, the impedance increases rapidly at the top end above 250MHz. This may seem OK if you are using a clock frequency of 200MHz, for instance, but as mentioned in previous columns, the impedance needs to be low up to the 5th harmonic, which is 1GHz in this case.

In Part 2, we will continue looking at the alternate approaches of analyzing the PDN. **PCBDESIGN**

References

1. Barry Olney, [Beyond Design: Power Distribution Network Planning](#) and
2. [Material Selection for SERDES Design](#)
3. Henry Ott, [Electromagnetic Compatibility Engineering](#)
4. Istvan Novak, [Quiet Power: Resonances in Power Planes](#)
5. Eric Bogatin, [Signal and Power Integrity - Simplified](#)
6. Johanson Dielectrics, [Basics of Ceramic Chip Capacitors](#)
7. Kemet, [SMT Capacitor Comparison](#)
8. X2Y, [Understanding capacitor inductance](#)
9. The ICD PDN Planner is available at www.icd.com.au



Barry Olney is managing director of In-Circuit Design Pty Ltd (ICD), Australia. ICD is a PCB design service bureau and specializing in board-level simulation. The company developed the ICD Stackup Planner and the ICD PDN Planner software. To read past columns or contact Olney, [click here](#).