

# **BOARD LEVEL SIMULATION SPECIALISTS**

**ICD Stackup Planner** - offers engineers/PCB designers unprecedented simulation speed, ease of use and accuracy at an affordable price

- 2D (BEM) field solver precision
- Characteristic impedance, edge-coupled & broadside-coupled differential impedance
- Unique field solver computation of multiple differential technologies per stackup
- Heads-up impedance plots of signal and dielectric layers
- User defined dielectric materials library - over 16,250 materials up to 100GHz

**ICD PDN Planner** - analyze multiple power supplies to maintain low impedance over entire frequency range dramatically improving product performance

- Fast AC impedance analysis with plane resonance
- Definition of plane size/shape, dielectric constant & plane separation for each on-board power supply
- Extraction of plane data from the integrated Stackup Planner
- Definition of voltage regulator, bypass/decoupling capacitors, mounting loop inductance
- Frequency range up to 100GHz
- Extensive Capacitor Library – over 5,250 capacitors derived from SPICE models

# Power Distribution Network Planning

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**SUMMARY:** *The power distribution network (PDN) of a multilayer PCB should distribute low noise and stable power to ICs over the entire board area. Ideally, the AC impedance, between power and ground, should be zero, up to the maximum operating frequency for reliable performance.*

Today's high-performance processors, with subnanosecond switching times, use low DC voltages with high transient currents and high clock frequencies in order to minimize the power consumption and hence, heat dissipated. Fast rise times, low output-buffer impedance and the simultaneous switching of busses create the high transient currents in the power and ground planes, degrading performance and reliability of the product. Inadequate power delivery can exhibit intermittent signal integrity issues. Also, many failures to pass electromagnetic compliance (EMC) are due to excessive noise on the PDN coupling into external cables and radiating emissions.

A typical high-speed design, incorporating DDR3 memory, contains five or six individual power supplies. The PDN must accommodate

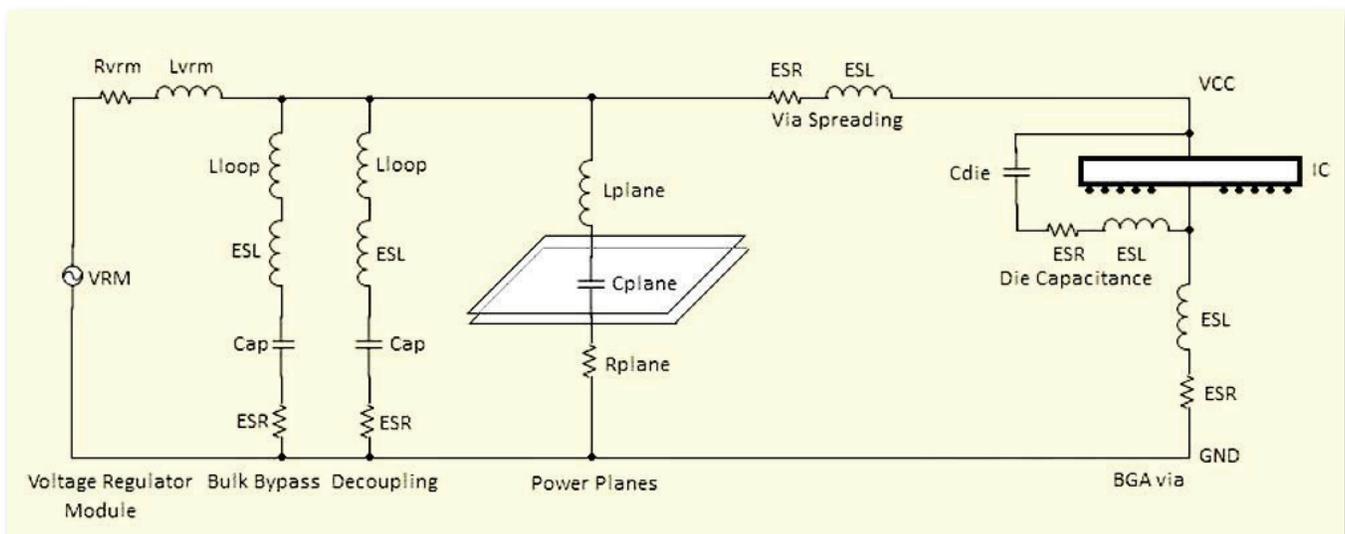
these variances of current drawn with as little change in power supply voltages as possible (5% voltage ripple is a typical requirement). So the goal of PDN planning is to design a stable power source, taking the above into account, for all the required power supplies. Ideally, the effective impedance of the PDN should be kept as low as possible, up to the maximum operating frequency.

PDN planning is a trade-off of cost/performance and results in the following:

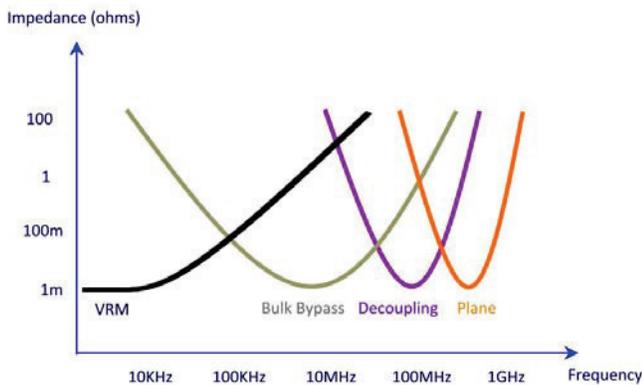
- Gives higher confidence in the performance and reliability of the product
- Meets the performance target at the lowest cost of production
- Finds and eliminates issues early in the design cycle

As with stackup planning, the PDN design is required before a single IC is placed on the board.

Figure 1 shows the topology of the PDN which includes the VRM, bulk bypass and decoupling capacitors, the plane, the die capaci-



**Figure 1:** PDN topology.



**Figure 2:** Impedance of VRM, capacitors and plane.

tance, plus BGA via and via spreading inductance.

Figure 2 illustrates the resonant frequency of the PDN components. Each component added to the PCB lowers the impedance of the PDN at a particular frequency. The PDN impedance for a computer-based product must be kept low and flat over a large frequency range for improved product performance. Each capacitor’s resonant frequency can be calculated by:

$$F_{res} = \frac{1}{2\pi\sqrt{LC}}$$

The first major component of the PDN is the voltage regulator module (VRM). The VRM is typically a switching regulator that adjusts the amount of current being supplied (via feedback) to keep the voltage constant at frequencies from DC to a few hundred KHz (depending on the regulator). For all transient events that occur at frequencies above this range, there is a time lag before the VRM can respond to the new level of demand.

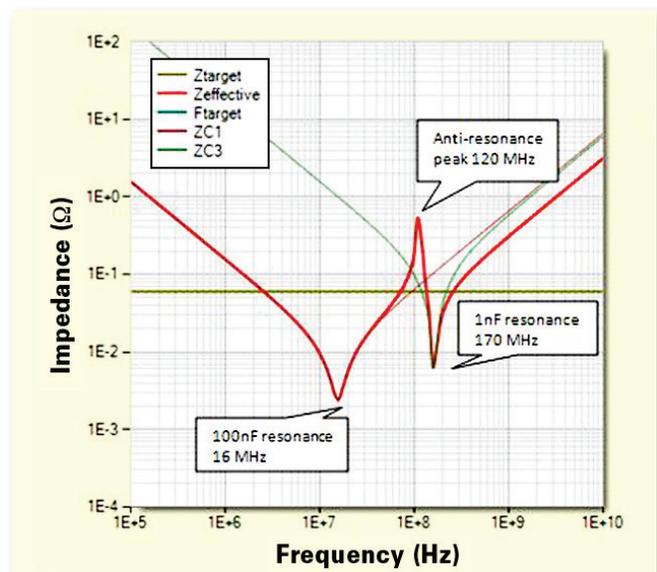
The second major component of the PDN is the bulk bypass (tantalum) and decoupling capacitors (ceramic). These capacitors supply instantaneous current (at different frequencies) to the drivers until the VRM can respond. In other words, it takes a finite amount of time for current to flow from the power supply circuit (whether on-board or remote) due to the inductance of the trace and/or leads to the drivers.

Every decoupling capacitor has an equiva-

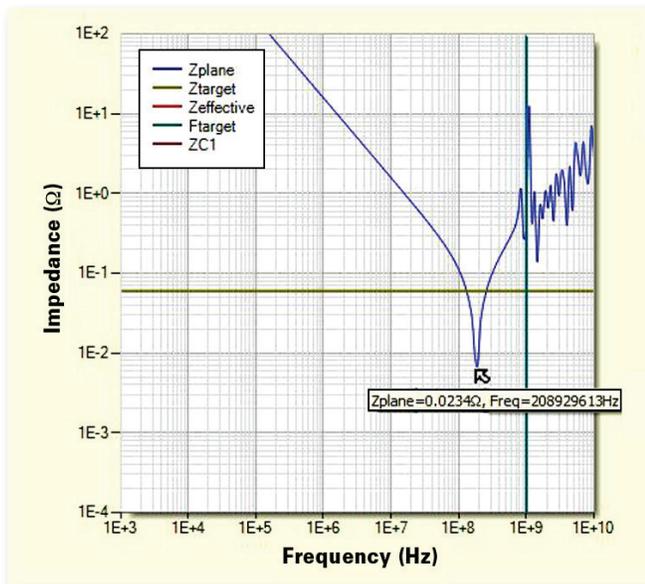
lent series inductance (ESL) which causes its impedance to increase at high frequencies. The bulk bypass capacitance provides low impedance, up to 10 MHz. High-frequency decoupling is provided by ceramic capacitors up to several hundred MHz, but above that only the third major component of the PDN—the plane capacitance itself—can reduce the PDN impedance. The power-to-ground plane capacitance of the PCB provides an ideal capacitor in that it has no series lead inductance and little equivalent series resistance (ESR), which helps reduce noise at extremely high frequencies.

Capacitors reach their minimum impedance at their resonant frequency, which is determined by the capacitance and the ESL. To meet the target impedance at a particular frequency, a capacitance value is chosen so that when mounted on the PCB, it will resonate at the desired frequency, and have an impedance that is equal to its ESR. Then, a sufficient number of those capacitors are placed in parallel so that the parallel ESRs approach the desired target impedance.

As one can see from Figure 2, each different value capacitor has a different resonant frequency. So one would assume that by placing many different values of capacitors on the board, the entire frequency range would be covered or have minimal impedance from DC to



**Figure 3:** Resonance and anti-resonance peaks for 10 of each 100 nF and 1 nF capacitors.



**Figure 4:** Plane resonance.

maximum frequency. Unfortunately, it is not as simple as that.

In Figure 3, we can see the resonant frequencies of the 100 nF and 1 nF capacitors being 16 MHz and 170 MHz, respectively. Where the 1 nF is capacitive (green trace sloping downward) and the 100 nF is inductive (brown trace sloping upward) intersect, they create a classic LC tank (parallel resonance) circuit raising the impedance at that point. This is called anti-resonance and appears each time a different value of capacitor is added to the network. It becomes obvious that in order to reduce the number of anti-resonance peaks we need to minimize the number of different value capacitors used in the PDN.

The effective decoupling capacitance area is not the capacitance of the entire board. Because of the velocity of propagation of electromagnetic energy, the effective area is only located within a finite radius of the IC. The radius of the effective capacitance area is given by:

$$r = vt = \frac{12t}{\sqrt{Er}}$$

Where  $r$  = radius (in),  $v$  = velocity of propagation,  $t$  = time in nS, and  $Er$  = dielectric constant

In FR-4,  $r$  is about 2.9 inches (74 mm). So for a large processor chip, capacitors can be placed within this radius around the outside of the chip. However, lower inductance is achieved by placing the capacitors as close as possible to the power pins.

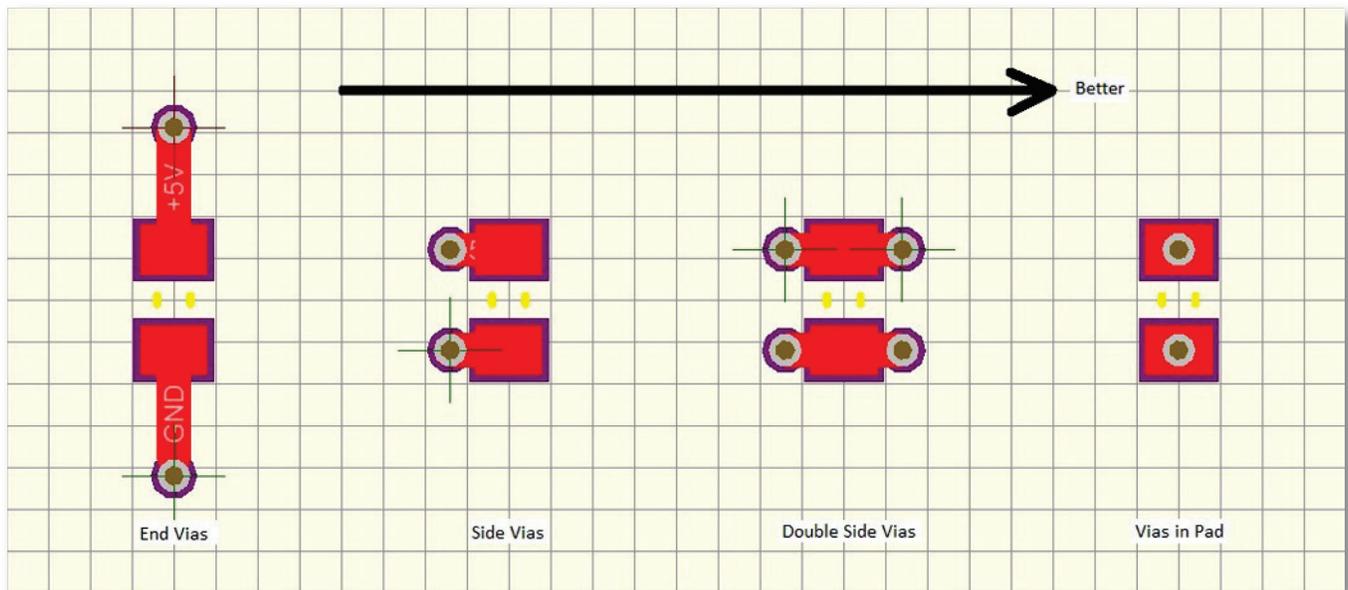
How many capacitors do we need? This depends on target impedance, which is calculated from the supply voltage, maximum current, transient current and maximum allowed ripple voltage for each power plane. This is where a good PDN analysis tool comes into play.

The resonance and anti-resonance peaks of the bypass and decoupling capacitors have been taken into account, but we also need to deal with the plane resonance. Ideally, the plane pair, a perfect lumped element capacitor of this size, should provide a very low impedance between power and ground at very high frequencies (several hundred MHz and higher). But planes, left open at the edges, behave like wide un-terminated traces, from a signal integrity point of view, reflecting at the ends and creating resonances in the transmission line.

The trough at 208 MHz in the plane (Figure 4) is the first resonance of the plane pair. As the frequency increases to half wavelength, the series resonance builds up a standing wave pattern reflecting from the open edges of the plane. Fortunately, this happens above 1 GHz. So for example, if we have DDR2 running at a fundamental of 400 MHz, we are operating well below this frequency.

Most of the inductance associated with bypass and decoupling capacitors is due to the mounting pad structure, the width of the trace from pad to via and the loop area to and from the planes. Inductance can be reduced by placing the vias close to each other and minimizing the length to the planes.

The mounted inductance or ESL of a capacitor is comprised of three components: capacitor footprint, capacitor height above or below the plane, and power plane spreading inductance. These three elements describe the loop in which current must flow: The bigger the loop, the more the inductance. The footprint (land pattern) for a capacitor dominates the ESL. It consists of via placement with respect to the pad, the length and width of traces connected



**Figure 5:** Capacitor mounting and via fanout.

to the pad, and the way the vias are connected to the power and ground planes. The location of the power/ground planes in the PCB stackup controls the height of the via. Inductance directly depends on the magnetic field, so reducing the energy associated with loop area reduces overall inductance.

Figure 5 illustrates 0402 capacitors with different fanout patterns. End vias are the worst-case where the loop area is the largest. This loop area can be reduced by placing the vias to the side and even more so by placing double vias either side of the pad, basically halving the inductance. The final case is that of via-in-pad. This reduces the loop area dramatically but caution should be used as not all assembly shops support this.

The second contributing factor to the inductance is the capacitor itself. The capacitor forms a part of the current loop, hence contributing to the inductance. Typically, a capacitor is made up of multiple plates connected alternately to the side posts. For a thicker capacitor, the current has to flow up and down and effectively increases the length of the current loop.

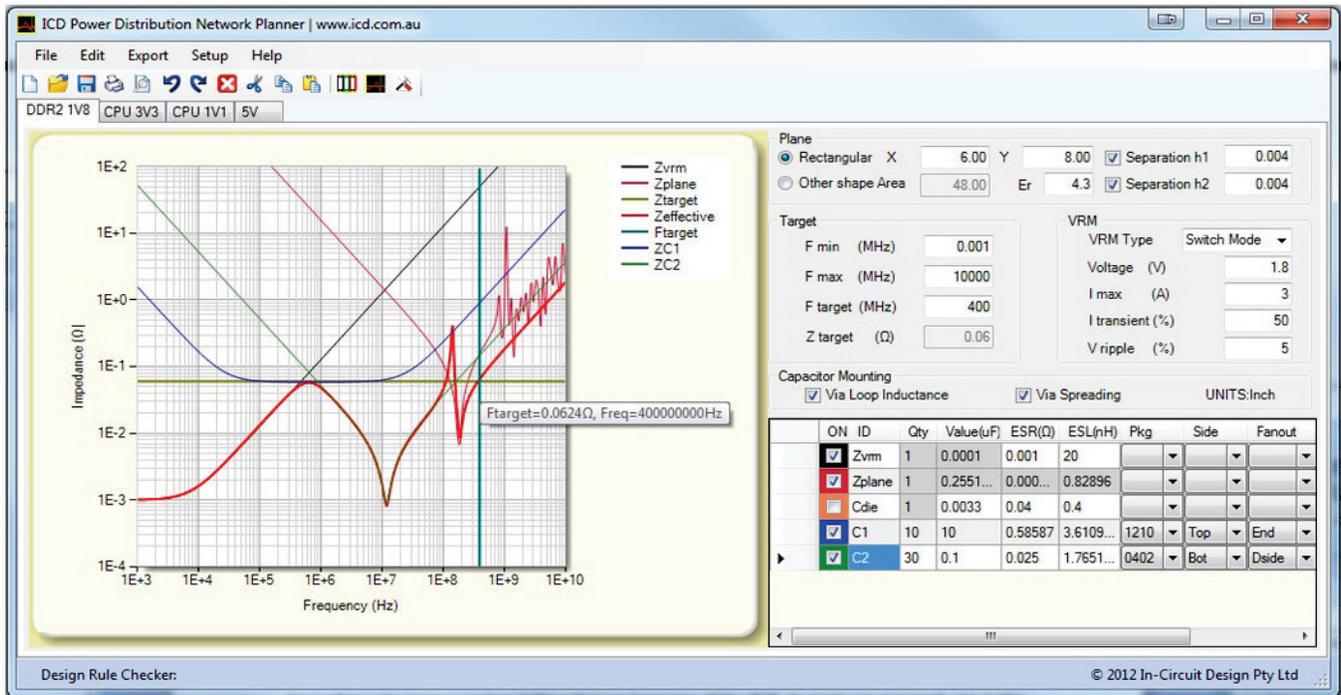
The inductance associated with current spreading into the power/ground planes also contributes to the total mounted inductance. Current in the planes becomes concentrated in the vicinity of the vias. Concentrated current

creates a higher magnetic field and therefore contributes to inductance.

Spreading inductance is higher at the edges and corners of the PCB. Current can approach vias in the middle of the board from four different directions, instead of two, when the capacitor is located at the corner of the board. It is therefore good practice to place the main processor in the center of the board as it elevates the spreading inductance issue and also opens channels for routing out to peripheral components. Also, the separation between the planes contributes to the spreading inductance.

In Figure 6, The ICD PDN Planner ([www.icd.com.au](http://www.icd.com.au)) illustrates the combined effect of the VRM, 10  $\mu$ F bulk bypass, 100 nF decoupling capacitors, the plane resonance of the board and capacitor mounting/loop inductance for a typical DDR2, 1.8V supply.

As mentioned, the objective is to keep the effective impedance as low as the target impedance (horizontal line) up to the fundamental frequency of the clock (400 MHz vertical line). In the above case, there is an anti-resonance peak at 158 MHz, but fortunately that is well below the clock frequency of 400 MHz. Also, one needs to keep the odd harmonics in mind. If the plane resonance appears at the 3<sup>rd</sup> (1.2 GHz), 5<sup>th</sup> (2 GHz) or 7<sup>th</sup> (2.8 GHz) harmonic, there could be an issue.



**Figure 6:** The ICD PDN Planner illustrates the PDN for 1.8V DDR2.

Points to remember:

- The PDN impedance for a computer-based product must be kept low and flat over a large frequency range for improved product performance
- In order to reduce the number of anti-resonance peaks, we need to minimize the number of different value capacitors used in the PDN
- Lower inductance is achieved by placing the capacitors as close as possible to the power pins
- Planes behave like wide unterminated traces, from a signal integrity point of view, reflecting at the ends and creating resonances
- Mounting/loop inductance can be reduced by placing the capacitors' vias close to each other and minimizing the length to the planes
- Place the main processor in the center of the board, as it elevates the spreading inductance issue and also opens channels for routing out to peripheral components
- A PDN planning tool is essential to

effectively analyze the PDN requirements and to ensure confidence in the performance and reliability of the product **PCB**

**References:**

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