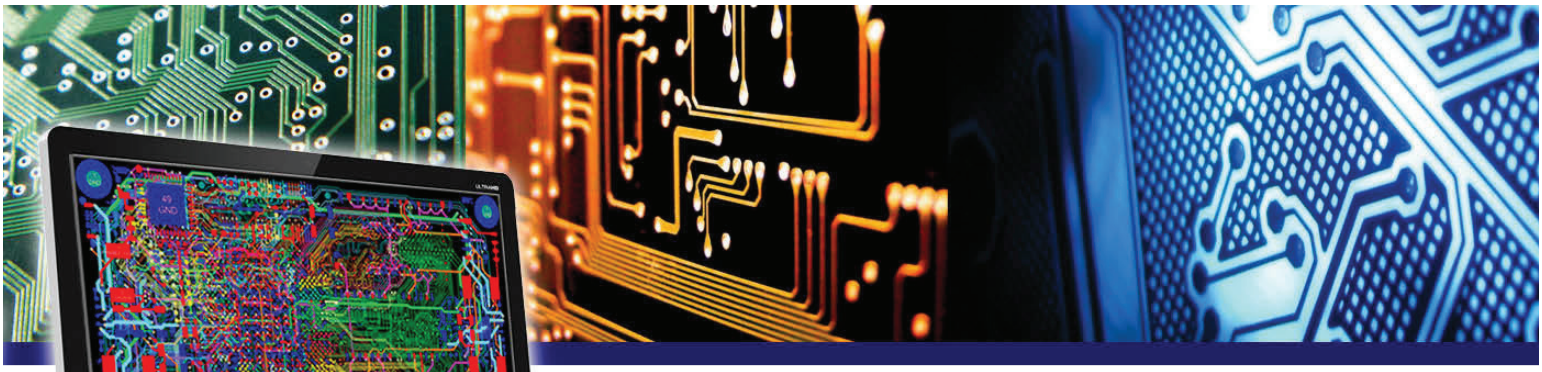

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Material Selection for SERDES Design

by Barry Olney
IN-CIRCUIT DESIGN PTY LTD | AUSTRALIA

Many challenges face the engineer and PCB designer working with new technologies. For SERDES—high-speed serial links—loss, in the transmission lines, is a major cause of signal integrity issues. Reducing that loss, in its many forms, is not just a matter of reducing jitter, bit error rate (BER) or inter-symbol interference (ISI). Materials used for the fabrication of the multilayer PCB absorb high frequencies and reduce edge rates thus putting the materials selection process under tighter scrutiny. This column will look at the factors that must be taken into account, in the selection process, and provides some options for PCB designers.

The ideal transmission line model has properties distributed along its length. A physical transmission line can be approximated by describing sections of signal and return path as a loop inductance along its length. The simplest equivalent circuit model, in Figure 1, has a series of capacitors separated by loop inductors. There are also small series resistors with the inductors and shunt resistors across the capacitors which we assume are negligible. If I recall from Circuit Theory 101, this looks very similar to a low-pass filter, which of course attenuates high frequencies.

The Fourier Theorem states that every function can be completely expressed as the sum of sine and cosine of various amplitudes and frequencies. The Fourier series expansion of a square wave is made up of a sum of odd harmonics. If the waveform has an even mark to space ratio then the even harmonics cancel. Also, as the frequency increases, the amplitude decreases.

A square wave can be expressed as:

$$F(t) = \cos(\omega t) - \cos(3\omega t)/3 + \cos(5\omega t)/5 - \cos(7\omega t)/7 + \cos(9\omega t)/9 \ldots\ldots$$

It can be observed in Figure 2, that the 9th harmonic (pink waveform) has the steepest slope. It is this component, of the square wave, that gives the overall square wave its fastest rise time.

A square wave is made up of a number of sinusoid waveforms of different frequencies. However, only the lower frequency components can transverse the transmission line reducing the rise time at the output. This rise time degradation is due to the losses in the transmission line (dielectric loss), which is frequency dependent, and is the main source of Inter-symbol In-

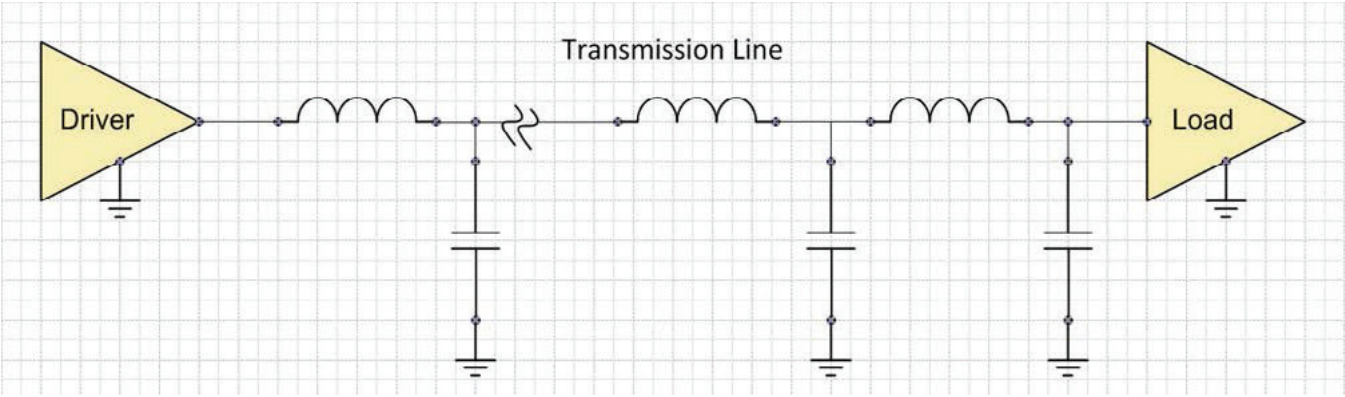


Figure 1. Ideal transmission line model.

MATERIAL SELECTION FOR SERDES DESIGN *continues*

terference (ISI). ISI is a significant contributor to jitter.

Analog designers, on the other hand, must be concerned about dielectric loss at low frequencies when constructing high-Q circuits intended to ring, without loss of signal amplitude, for recurring cycles.

FR-4, the glass epoxy material commonly used for multilayer printed circuit fabrication, has negligible loss at frequencies below 1GHz. But since the dielectric loss is frequency-dependent, at higher frequencies, the dielectric loss of FR-4 increases. So, for higher frequency digital, RF and microwave design alternative materials that exhibit lower losses need to be considered.

Designed for use in high density multilayer boards, FR-4 is suitable for surface mount components, multi-chip modules, direct chip attachment, automotive and wireless communications. FR-4 (flame retardant) has a low glass transition temperature (Tg) ~135°C and is mostly used for thin PCBs of 62 mil. FR-4 is also available with a high Tg > 170°C and is used on thicker PCB > 62 mils. The characteristics of FR-4 also make it particularly beneficial in high volume, fine-line, multilayer applications.

For digital applications below 1GHz, the losses can be ignored. But what is the highest frequency that needs to be considered? The maximum bandwidth of a signal is not determined by the fundamental frequency but rather by the rise time of the signal. Since the harmonics of the fundamental signal determine the rise time of the signal, then it is the maximum frequency harmonic that must be considered. I typically use the 5^{th} harmonic but it may be the 7^{th} if the rise time is extremely fast. So, for a 400MHz, fundamental frequency, the 5^{th} harmonic is 2GHz.

At frequencies above 1GHz, the main selection criteria for PCB fabrication material is dielectric Loss or loss tangent (Df) and glass transition temperature (T_g). Df is a parameter of a dielectric material that quantifies its inherent dissipation of electromagnetic energy. The term refers to the tangent of the angle in a complex plane between the resistive (lossy) component of an electromagnetic field and its reactive (lossless) component. Standard FR-4 has a Df of 0.02 whereas a low loss dielectric may have < 0.001 at 10GHz.

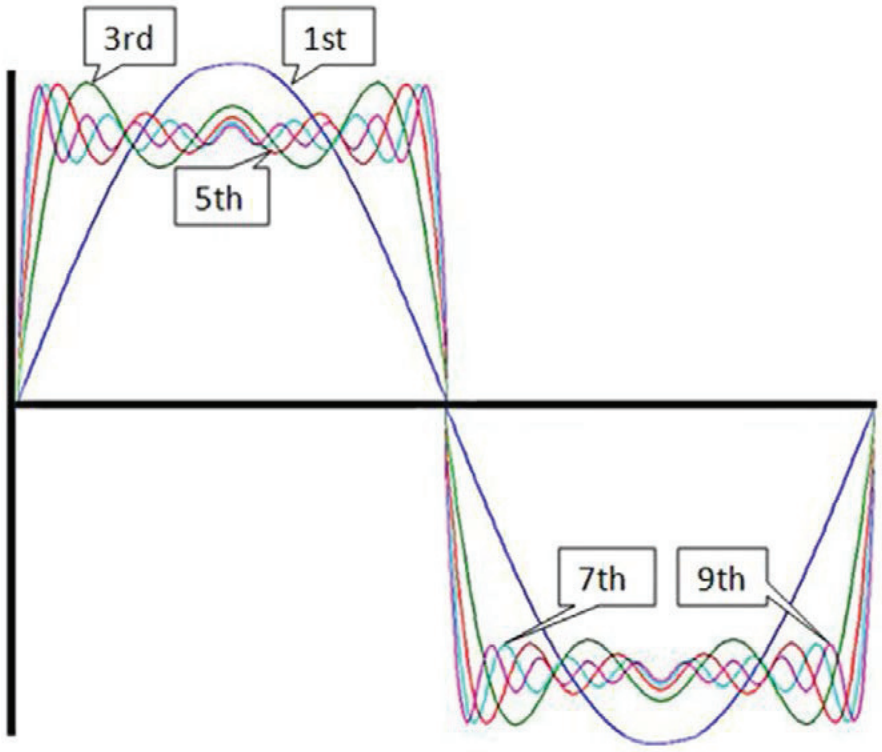


Figure 2. Reconstruction of a square wave using the odd harmonics.

The glass transition temperature is the point at which a glassy solid changes to an amorphous resin/epoxy. If the temperature exceeds the T_g, the material rapidly expands in the Z-axis. Plus, mechanical material properties degrade rapidly—strength and bonds in the material. A high T_g guards against barrel cracking and pad fracture during reflow. Standard FR-4 has a T_g of 135-170°C whereas the high-speed materials are generally over 200°C.

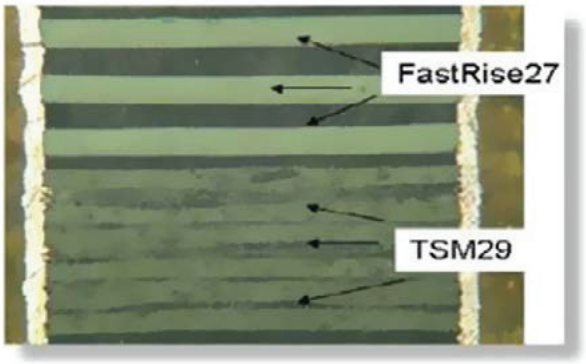
Also, at high frequencies, a non-uniform dielectric in the substrate can cause skew in differential signals. The inconsistency of the dielectric material comes from that fact that

the fiberglass and the epoxy resin, that make up PCB core (laminate) and prepreg materials, have a different dielectric constant. And, because the fabricator cannot guarantee the placement of the fiberglass with respect to the location of the traces, this results is uncontrolled differential skew. One way to avoid this is to always route differential pairs diagonally, across the board, as the fiberglass matting is laid in the X, Y direction. Or, zigzag diagonally across the board. Alternatively, a fiberglass-free material, such as fastRise™27, can be used to eliminate differential skew. However, fiberglass free materials come at a price.

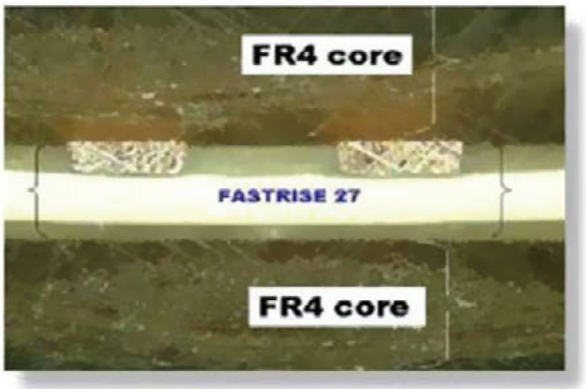
The Taconic TSM-DS family of cores combined with fastRise27 (Df: 0.0014 @ 10 GHz) prepreg is an industry leading solution for the lowest possible dielectric losses that can be attained at epoxy-like (200 - 215°C) fabrication temperatures. For high-speed multilayer PCBs, the price of poor yield drives up the final material cost. fastRise27 enables the sequential lamination of TSM-DS, at low temperature, with consistency and predictability that reduces cost according to Taconic.

Another attribute of dielectric materials is the dielectric constant or relative permittivity (E_r or Dk) that reflects the extent to which it concentrates electrostatic lines of flux. It is the ratio of the amount of electrical energy stored in a material by an applied voltage, relative to that stored in a vacuum. If a material with a high dielectric constant is placed in an electric field, the magnitude of that field will be measurably reduced within the volume of the dielectric. Therefore, a lower E_r is desirable for high-frequency design.

Park Electrochemical Corporation, for instance, produces Nelco 4000-13 laminates that use NE-glass rather than the default E-glass. The dielectric constant for NE-glass is lower than E-glass—hence, the difference in E_r between resin and glass is low, which leads to less skew. NE-glass shows better temperature stability, lower E_r, and lower loss than the equivalent E-glass. The reduced E_r and dissipation factor yields important signal integrity benefits in high-speed signaling applications.



Multiple plies of *fast*Rise™27 form flat planar structures. This photo shows the contrast between fiberglass reinforced TSM-29 and non-reinforced *fast*Rise™27.



***fast*Rise™27 fiberglass free prepreg eliminates skew in differential traces. Here the contrast between the black FR-4 layer with a high glass content and the fiberglass free *fast*Rise™ prepreg is shown.**

Figure 3. Image of fastRise27 fiberglass-free prepreg eliminates differential skew. (Courtesy of Taconic)

MATERIAL SELECTION FOR SERDES DESIGN *continues*

Close attention should also be paid to the skew associated with the fiber weave effect. For high-speed data rates of 5 Gbps and above, this skew significantly cuts into the available jitter unit interval (UI) budget and leads to a reduction in the observed eye width at the receiver. If the flexibility exists, specify a denser weave material (2113, 2116, 1652 or 7628) compared to a sparse weave (106 and 1080). Figure 4 compares the different types of fiberglass weaves to a 4/4 mil differential pair. Notice that one side of the pair can be routed over the fiberglass and the other over the gap (resin), depending on the placement. The different dielectric constants create skew. Routing the differential signals diagonally across the weave can reduce this skew considerably.

DC blocking capacitors are common sources of impedance discontinuities in high-speed serial channels. Typically, narrow trace width and narrow trace spacing are used to construct the 100 ohm differential transmission line pair. However, as these narrow trace pairs are routed into the surface mount pads of a DC blocking capacitor, the sudden widening of the controlled impedance traces as they join with the capacitor pads can cause an abrupt impedance discontinuity. The effect of this discontinuity appears as excess capacitance because the surface mount pads of the DC blocking capacitors act as a parallel plate with the reference plane underneath.

To remove the excess parasitic capacitance associated with surface mount pads, remove a portion of the reference plane that is directly beneath the surface mount pads. This allows the signal that traverses through the DC blocking capacitor to reference a lower plane (further away) and reduces the parasitic capacitance, thereby minimizing the impedance mismatch. The optimum routing structure has a 20–25 mil wide cutout, under the capacitor lands, depending on the distance to the lower plane.

With so many materials to choose from which are the best for your specific product? Low cost generally means low quality. But the price of poor yield drives up the final material cost. And different materials are available locally compared to offshore. Typically, prototype boards are fabricated locally whereas for mass production, Asia is more economical.

The ICD Dielectric Material Library in Figure 5 has recently been upgraded to include over 5,650 materials many of which are suitable for high-speed, RF and microwave design up to 40GHz.

With the continuous trend to smaller feature sizes and faster signal speeds, planar capacitor laminate or embedded capacitance materials (ECM) are becoming a cost-effective solution for improved power integrity. This technology provides an effective approach for decoupling high-performance ICs whilst also reducing electromagnetic interference.

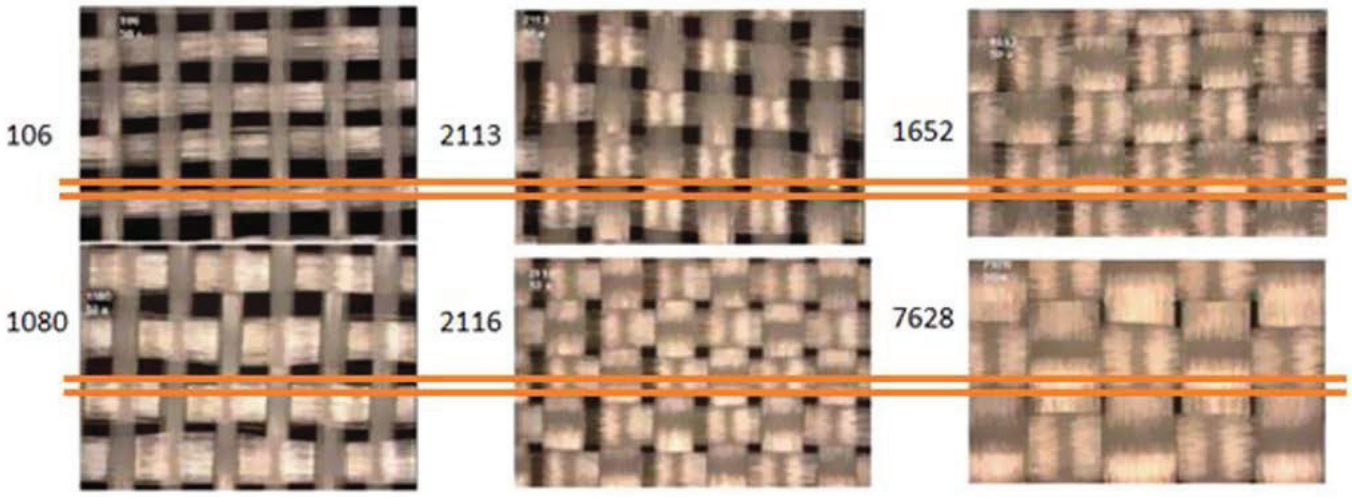


Figure 4. Different types of fiberglass weaves compared to a differential pair. (Courtesy of Altera)

Standard	Df	High-speed	Df	Ultra high-speed	Df
Panasonic Hiper V	0.0240	Isola FR408	0.0090	Isola I-Speed	0.0065
Isola IS415	0.0230	Isola FR408HR	0.0086	Nelco N4800-20SI	0.0060
Isola 370HR	0.0210	Nelco N4000-13	0.0080	Nelco Meteorwave 1000	0.0055
Panasonic FR-4	0.0190	EMC EM-888 *	0.0080	Nelco Meteorwave 2000	0.0040
ITEQ IT-180A *	0.0170	Panasonic Megtron 4	0.0080	Rogers RO4450B	0.0040
Isola FR406	0.0163	Ventec VT-464(LK)	0.0080	Rogers RO4350B	0.0037
Nelco N4000-29	0.0160	Nelco N4000-13SI	0.0070	Rogers RO3001	0.0030
EMC EM-355(D) *	0.0150	Nelco N4800-20	0.0070	Isola I-Tera	0.0028
Panasonic Hiper F	0.0150	Isola IS620i	0.0070	Panasonic Megtron 6	0.0020
Doosan DS-7809	0.0150			Taconic fastRise27	0.0014
Doosan DS-7408	0.0140			Taconic TSM-26	0.0014
Technolam FR-4 86UV *	0.0130			Taconic TSM-30	0.0013
EMC EM-828 *	0.0120			Rogers RT/Duriod 5870	0.0012
NanYa Plastics NP-175TL *	0.0120			Taconic TSM-DS/DS3	0.0010
Panasonic Megtron 2	0.0100			Rogers RT/Duriod 5880	0.0009
Ventec VT-464	0.0100				

Table 1. Materials available in the ICD Dielectric Materials Library—Dielectric Loss @ ≤ 10GHz (A full list of materials and properties is available from www.icd.com.au).
* Taiwanese materials available in Asia

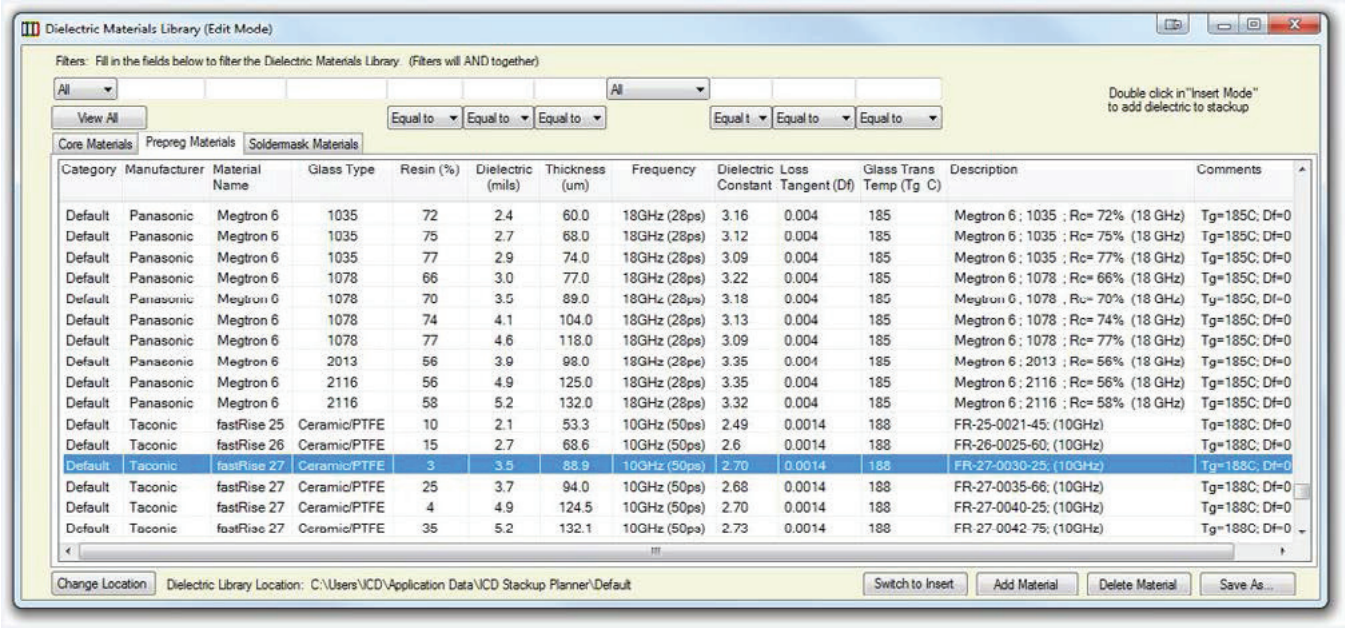


Figure 5. ICD Stackup Planner—Dielectric Materials Library with over 5,650 materials up to 40GHz.

MATERIAL SELECTION FOR SERDES DESIGN *continues*

Embedded capacitance technology allows for a very thin dielectric layer (0.24–2.0 mil) that provides distributive decoupling capacitance and takes the place of conventional discrete decoupling capacitors over 1GHz. Unfortunately, standard decoupling capacitors have little effect over 1GHz and the only way to reduce the AC impedance of the power distribution network above this frequency is to use ECM or alternatively die capacitance. These ultra-thin laminates replace the conventional power and ground planes and have excellent stability of dielectric constant and loss up to 15GHz.

The ZBC-2000 laminate is constructed using a single ply of either 106 or 6060 style prepreg, yielding a dielectric thickness after lamination of 2 mil, when measured by cross-sectioning. The ZBC-1000 technology results in a 1 mil dielectric distributed capacitance material. FaradFlex™ and Interra™ buried capacitance products utilize a durable resin system for non-reinforced dielectrics for 1 mil thickness and below. Also with a product range up to 20nF per square inch in capacitance density, 3M ECM is the highest capacitance density embedded capacitance material on the market.

Zeta Lam allows significant layer count reduction in PCBs with better signal performance. Having a low dielectric constant combined with very high withstanding voltage, these glass free films change the design rules for via diameter and trace width, while still conforming to the manufacturing needs of the PCB shop. Three traces between vias at a 0.4 mm pitch is not only possible but very manufacturable according to Integral Technology.

For high-speed serial link performance, reliability and production yields are of greater importance than cost. But unless you are pushing limits of the technology, then a dielectric material of Df < 0.01 will most likely suffice.

Points to remember

- A transmission line looks very similar to a low-pass filter—which of course attenuates high frequencies
- A square wave is made up of a number of sinusoid waveforms, of different frequencies, however only the lower frequencies components can transverse the transmission line
- FR-4 has negligible loss at frequencies below 1GHz. But since the dielectric loss is frequency-dependent, at higher frequencies the dielectric loss of FR-4 increases
- The maximum bandwidth of a signal is not determined by the fundamental frequency but rather by the rise time of the signal—5th harmonic
- At high frequencies, a non-uniform dielectric in the substrate can cause skew in differential signals
- A fiberglass-free material such as fastRise27 can be used to eliminate differential skew

Manufacturer	Material	Description	Thickness (mil)
3M	ECM	Embedded capacitance material	0.24, 0.47, 0.55
DuPont	Interra HK04	Ultra thin laminate	0.5, 1.0
Integral Technology	Zeta Bond	High T_g epoxy based adhesive film	1.0, 1.5, 2.0
Integral Technology	Zeta Lam SE	Low CTE C-stage dielectric with a Hi T_g	1.0
Integral Technology	Zeta Cap	Hi performance polymer coated copper	1.0
Oak-Matsui Technology	FaradFlex	Planar capacitor	0.31,0.47,0.63,0.94
Sanmina	ZBC1000	Buried cap, hi performance decoupling	1.0
Sanmina	ZBC2000	Buried cap, hi performance decoupling	2.0

Table 2. Embedded capacitor materials available in the ICD Dielectric Materials Library.

• Close attention should be paid to the skew associated with the fiber weave effect

• Specify a denser weave material (2113, 2116, 1652 and 7628) compared to a sparse weave (106 and 1080)

• DC blocking capacitors are common sources of impedance discontinuities in high-speed serial channels. The optimum routing structure has a 20–25 mil wide cutout, under the capacitor lands, depending on the distance to the lower plane.

• Planar capacitor laminate or embedded capacitor materials are becoming a cost-effective solution for improved power integrity. **PCBDESIGN**

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The ICD Stackup and PDN Planner can be downloaded from www.icd.com.au

Barry Olney is managing director of In-Circuit Design Pty Ltd (ICD), Australia. ICD is a PCB design service bureau and specializing in board-level simulation. The company developed the ICD Stackup Planner and the ICD PDN Planner software. To read past columns or contact Olney, click here.