

# BOARD LEVEL SIMULATION SPECIALISTS

ICD Stackup Planner - offers engineers/PCB designers unprecedented simulation speed, ease of use and accuracy at an affordable price

- 2D (BEM) field solver precision
- Characteristic impedance, edge-coupled & broadside-coupled differential impedance
- Unique field solver computation of multiple differential technologies per stackup
- Heads-up impedance plots of signal and dielectric layers
- User defined dielectric materials library - over 16,250 materials up to 100GHz

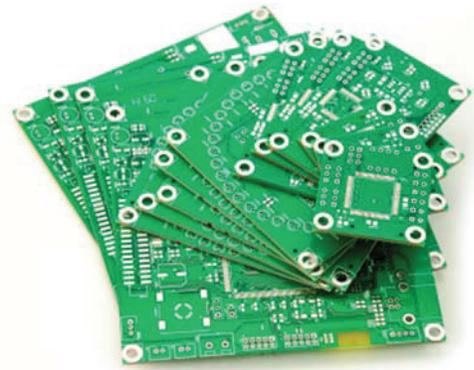
ICD PDN Planner - analyze multiple power supplies to maintain low impedance over entire frequency range dramatically improving product performance

- Fast AC impedance analysis with plane resonance
- Definition of plane size/shape, dielectric constant & plane separation for each on-board power supply
- Extraction of plane data from the integrated Stackup Planner
- Definition of voltage regulator, bypass/decoupling capacitors, mounting loop inductance
- Frequency range up to 100GHz
- Extensive Capacitor Library – over 5,250 capacitors derived from SPICE models

# Introduction to Board Level Simulation and the PCB Design Process

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IN-CIRCUIT DESIGN PTY LTD | AUSTRALIA



**SUMMARY** — *Board-level simulation reduces costs by identifying potential problems at the conceptual stage, so that they can easily be avoided, and then catching any further issues, during the design process, eliminating the potentially disastrous final stage changes.*

High-speed digital multilayer boards can be designed to work right the first time, with little additional effort, providing you follow a tried and proven process that results in a reliable, manufacturable design that conforms to specifications and is produced on time and to budget.

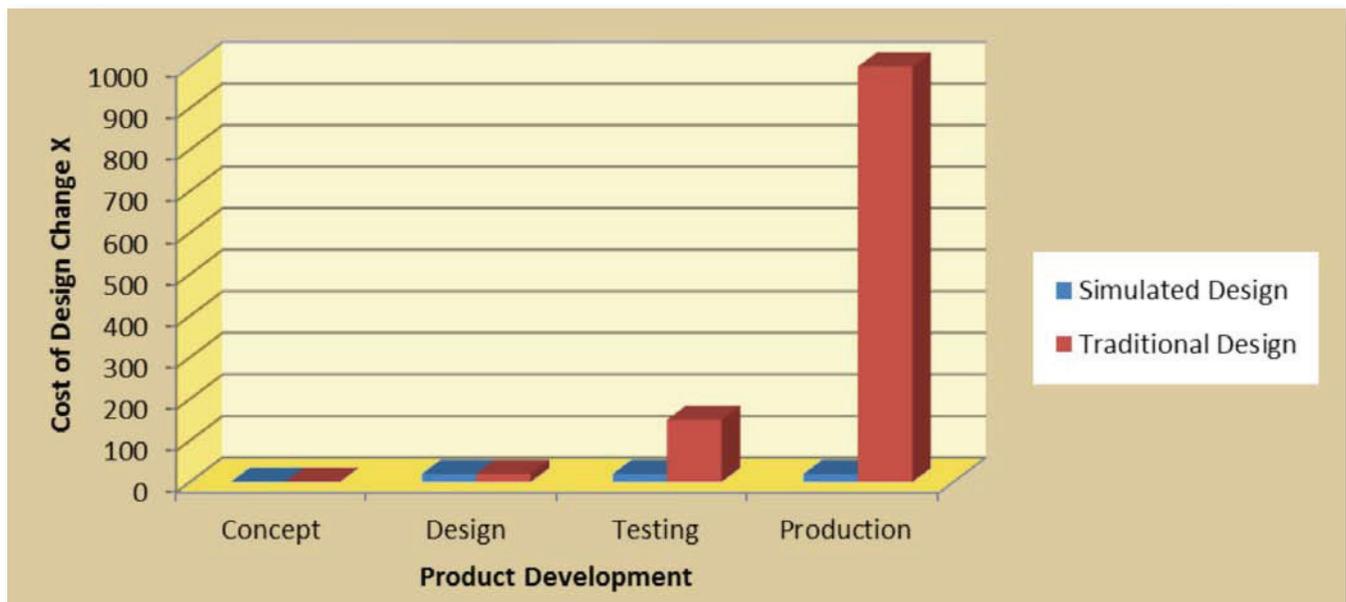
Typically, a high-speed, computer-based design takes three iterations to develop a working product. However, the product life cycle these days is very short, and therefore, time-to-market is of essence. One board iteration can cost more than \$25K. And this is only in engineering time and does not consider the cost of de-

laying the products' market launch. This missed opportunity could cost hundreds of thousands of dollars.

If changes are made late in the design process, then it takes more time, people, material and therefore, money. The idea of board-level simulation is to identify issues early in the design process and rectify them before they become a major problem.

As seen in Figure 1, design changes that occur in the conceptual stage cost nothing; during the design stage requires just a little extra time; during the test stage means that you have to go back one stage and re-design; and design changes during production, or worse still, in the field, can cost millions to fix and possibly damage the company's reputation.

This is where board-level simulation cuts costs: By identifying potential problems at the conceptual stage so that they can easily be avoided, and then catching any further issues



**Figure 1:** The cost of design change during the product development.

during the design process, which eliminates the potentially disastrous final stage changes. Of course, we also need to keep our eye on the ball during the entire design process by catching any small issue before it becomes a major problem.

Board level simulation and the design process cover the following:

1. Stackup planning
2. PDN planning
3. Design rules and DFM
4. Pre-layout simulation
5. Mixed analog digital technologies
6. Critical placement
7. Interactive placement and routing strategies
8. Critical routing
9. Post-layout simulation (already done)

I will be reviewing these topics in more detail over the coming months, but here are some initial factors to consider for each:

### 1. Stackup Planning

The configuration of the PCB stackup depends on many factors, but whatever the requirements, one should ensure that the following rules are followed in order to avoid a possible debacle.

- All signal layers should be adjacent to, and closely coupled to a reference plane, creating a clear return path and eliminating broadside crosstalk.

- Good interplane capacitance to reduce inductance at high frequencies.

- High-speed signals should be routed between the planes to reduce radiation.

- The substrate should be symmetrical with an even number of layers, which prevents the PCB from warping during manufacture and reflow.

- The stackup should accommodate a number of different technologies.

It is not always possible to configure the stackup to have both tight coupling of the planes and tight coupling of the signal layers to the planes, as this depends on the number of layers and the available materials. Four- and six-layer boards typically have this issue. Fortu-

nately, the lower layer count boards are generally used for designs below 100 MHz so the interplane capacitance may not be so important at these frequencies.

It is imperative that we plan the board stackup from the beginning, ensuring that both single-ended and differential impedances conform to the technology requirements. And, be sure to ensure that the selected materials are available from our chosen fabrication shop — this step is regularly missed. Changing the stackup towards the end of the design process could mean changing trace widths and clearances to achieve the correct impedance, which could create a lot of unnecessary work.

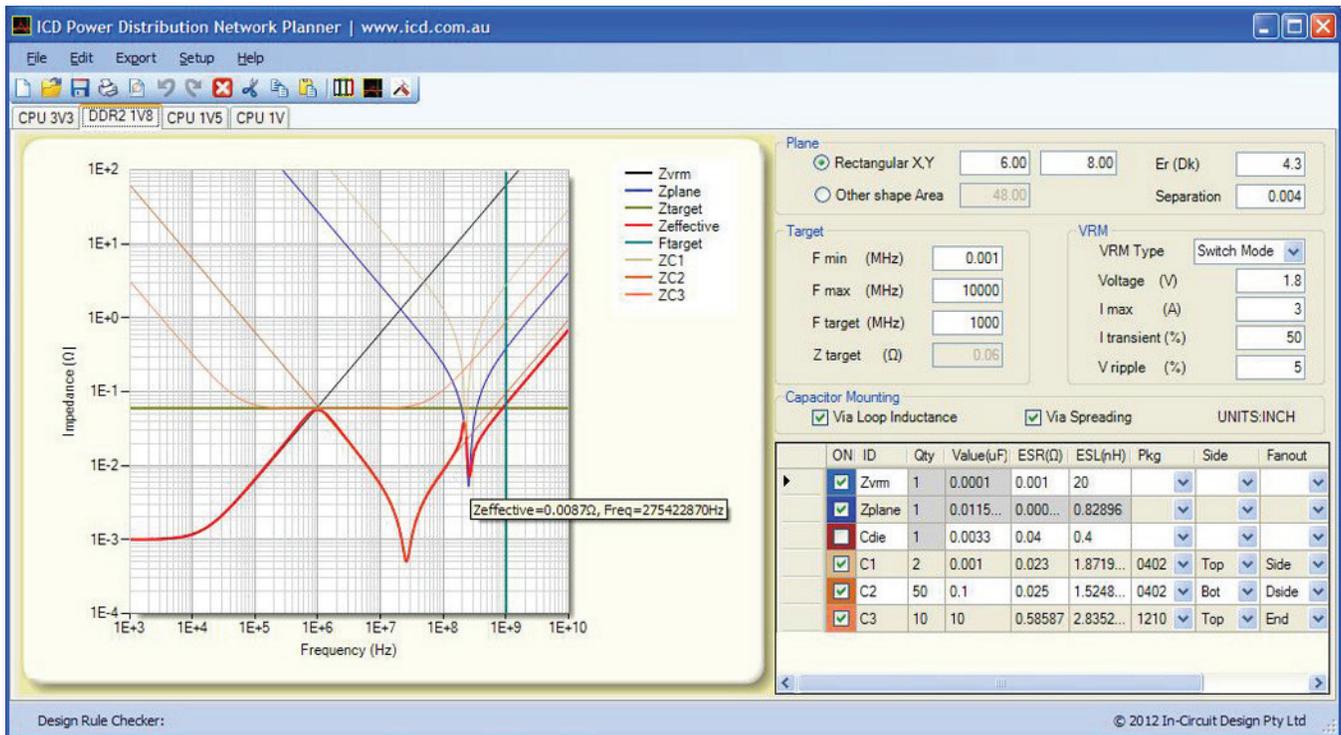
At this stage we need to plan where the power planes will be in the stackup, considering that every signal layer needs to have a reference plane (either ground or power) adjacent to it in order to provide a clear return path.

### 2. PDN Planning

The design of the power distribution network (PDN) is also a very important part of the conceptual design process, ensuring that we have a stable power delivery system before we even start placing a chip on the board.

The idea of AC analysis of the PDN is to keep the effective impedance of the PDN as low and flat as possible over the required frequency range for reliable product performance. A switch mode voltage regulator module (VRM) provides low impedance up to about 30 KHz. Then, bypass tantalum capacitors lower the impedance up to about 10 MHz. Ceramic capacitors then provide high-frequency decoupling up to several hundred MHz. The power-to-ground plane capacitance of the PCB provides an ideal capacitor in that it has no series lead inductance and little equivalent series resistance (ESR), which helps reduce noise at extremely high frequencies.

This is a trial-and-error process and needs to be done with the assistance of an analysis tool. The ICD PDN Planner (available for download from [www.icd.com.au](http://www.icd.com.au)) in Figure 3 illustrates a typical decoupling scheme showing how the VRM, capacitors and the planes are used to reduce the effective impedance of the PDN.



**Figure 2:** The ICD PDN Planner illustrates a typical decoupling scheme for 1.8V DDR2.

### 3. Design Rules and Design for Manufacturability (DFM)

Design rules should be set up and attached to critical nets in the schematic. This allows the engineer to transfer his desired intent, with regard to placement and routing, to the PCB designer without the information being lost in the process. One should keep in mind that if rules are modified in the PCB database then they need to be back-annotated to the schematic or they may be lost.

Design rules should be based on the manufacturer's device specifications and the relevant industry documents and standards that are available. For instance, DDR2 specifications (JESD79-2E) can be downloaded from JEDEC. Also, there are design guides and design technique documents available for download from Micron, Xilinx, Altera, etc., which are very helpful.

The IPC-2220 series of design documents, developed over the years by the industry, contain essential information for the design of SMT and mixed-signal multilayer boards and should be used to set up the basic design rules ([www.ipc.org](http://www.ipc.org)).

The technology rules are based on the minimum pitch of the BGA components employed and are basically the largest trace, clearance and via allowable whilst minimizing PCB fabrication costs.

Once these rules have been established, calculate the stackup required for the desired characteristic impedance ( $Z_0$ ) and the differential impedance ( $Z_{diff}$ ). These are typically  $Z_0 = 50$  ohms and  $Z_{diff} = 100$  ohms. The ICD Stackup Planner can be used for these calculations. Keep in mind that lower impedance will increase the  $di/dt$  and dramatically increase the current drawn (not good for the PDN); higher impedance will emit more EMI and also make the design more susceptible to outside interference. So, a good range of  $Z_0$  is 50 - 60 ohms.

Design for manufacturability (DFM) is the practice of designing board products that can be produced in a cost effective manner using existing manufacturing processes and equipment.

DFM is gaining more recognition as it becomes clear that the cost reduction of printed circuit assemblies cannot be controlled by manufacturing engineers alone. The PCB designer

now plays a critical role in cost saving and the DFM needs to be practiced throughout the entire design process. Again, identifying an issue too far into the process can cost time and money.

**4. Pre-Layout Simulation**

Pre-layout simulation allows the designer to predict and eliminate signal integrity, crosstalk and EMC issues early in the design process. This is the most cost effective way to design a board with fewer iterations rather than starting with the post-layout simulation.

One can quickly simulate complex interconnect scenarios including integrated circuits, transmission lines, connectors and passive components and identify which scenario is best suited to a particular design.

The value and placement of the series resistors and VTT pull-ups for data, address and command nets depends on the distances between the loads, number of loads and the stackup of the board, and are best determined by simulation. The series terminator may not be required if a single memory chip is used and the trace length is short.

**5. Mixed Analog and Digital Technologies**

In the past, we have only had to deal with mixed analog and digital technologies, but radio frequency (RF) and analog mixed-signal (AMS) technologies, which serve the rapidly growing wireless communication market, are essential in today's PCB design. A digital system is also an RF system with significant noise and therefore interference potential.

Digital technologies with different voltage levels can also cause interfere with each other. The technology being used has changed quite dramatically over the years, from TTL devices

(with high thresholds) to today's high-speed Gb/s devices (with noise margins as low as 500mV). The trend is toward lower processor core voltages, which conserves power. But, reducing the core voltage also reduces maximum operating frequency and the level of acceptable crosstalk.

In analog circuits, external noise sources are usually the primary concern. However, in digital circuits, the internally generated noise sources are of major concern.

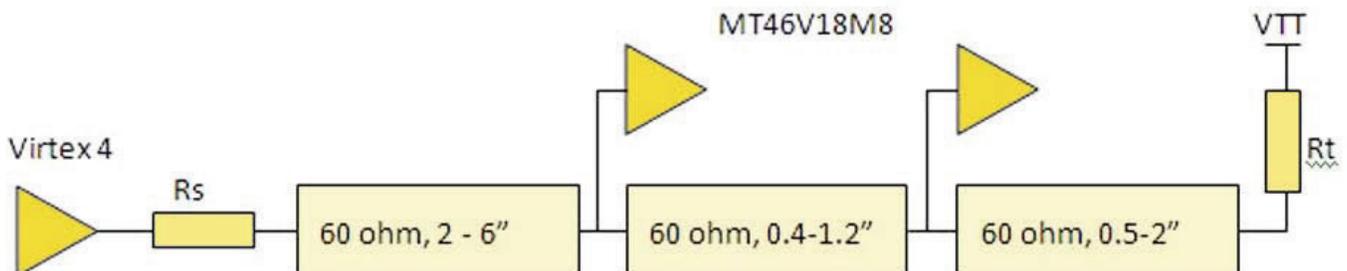
When planes are used to distribute power supplies, crosstalk (coupling) can occur through the ground return path for these signals. This is called common-mode impedance coupling. Essentially, a returning signal causes a ground potential rise due to the DC resistance of the plane. This problem can be very significant, especially in analog circuitry when digital signals are present.

Although a single-point ground may be desirable in low-frequency analog circuits, it may be the primary source of noise coupling and emissions in a digital circuit. When mixed analog and digital circuits are used on the same PCB, the best approach, for grounding practices is to use one solid and common ground plane and ensure that the routing of the traces does not create crosstalk.

**6. Critical Placement**

To obtain an excellent route completion rate on a complex design, placement is extremely important. If the board is difficult to route, it may just be the result of poor placement.

The pre-layout simulation of high-speed signals gives us an advantage when it comes to placement. The critical nets must be of a certain length. For instance, the pre-layout simulation



**Figure 3:** Example of DDR2 data signals simulated to find the best placement and routing strategy.

might suggest that a balanced T section route of 1.5 inches on all address, command and control lines of our DDR2 memory would be the best approach, and that data and strobes be no more than 1.2 inches matched to within 25 mils. Obviously, this does not give us much room to play with, so the correct positioning of these devices initially is of paramount importance. Placing the processor in the centre of the board allows all signals to be fanned out and promotes star wiring which is best for high-speed signals.

### 7. Interactive Placement and Routing Strategies

When the engineer creates the schematic he does so in logical, functional blocks — and that is exactly the way we should place and route the PCB. Cross-probing between the schematic and PCB database can be done in all major EDA packages and is recommended for design integrity.

For example, I often see PCB designers randomly placing resistors on the board. It is only a resistor — or is it? Well, that resistor could be a static pull-up that can be placed anywhere within reason or it could be a series terminator for a high-speed signal that needs to be placed within 200 mils of the driver. One should know the function of every component in order to make a valued decision with regard to effective placement, and cross-probing achieves this.

Critical placement should (of course) be done first. Then position the highest frequency components nearest the connectors and graduate the placement from high to low speed devices, with the low frequency analog devices positioned farthest from the connectors in a corner. Highlight the components on the schematic and move them into position on the PCB, one by one, making sure that you have the entire functional block in the one area. This is a tedious process, but it is the only way to ensure the placement is optimum.

Interactive routing is done in much the same way. Firstly, cross-probe and select the critical signals from the schematic, fanout, and route on the board. Route in priority from the most critical to least critical nets. I often use the autorouter to finish off the non-critical nets, but this of course depends on the quality of the

autorouter. I certainly would not attempt this with a basic router.

### 8. Critical Routing

I previously mentioned that the pre-layout simulation determines the placement of the critical components which in turn determines the critical routing topology. So, it is a simple process once you have the design methodology right, although at times one loses a bit of hair when tuning nets to length. Having so many matched-length signals on the size of a postage stamp is a daunting thought.

For DDR designs, differential clocks should be routed first, because all other signal lengths/delays are referenced to tClk, followed by data and strobe signals. Next, route the address, command and controls signals. It is best, although the pre-layout simulation has given us a routing strategy, to route a couple of each signal group first, then run the post-layout simulator to check the waveforms, skew and radiation on this sample group before continuing with the routing. The pre-layout simulation gives us a good heads-up, but the physical board simulation can be quite different in some cases.

### 9. Post-layout Board Level Simulation

A preliminary batch mode simulation is initially completed on the design. Default IC characteristics, crosstalk of 150mV maximum and EMC to FCC, CISPR Class A and B are set up in the simulator. The batch mode simulation automatically scans large numbers of nets on an entire PCB, flagging signal integrity, crosstalk and EMC hot spots.

The post-layout simulation analysis can then be prepared using supplied specifications. This is an extensive interactive board level simulation which takes the analysis to the next level — simulating trouble spots identified by the batch analysis in order to further resolve the issues with greater accuracy.

Crosstalk is typically picked up on long, parallel trace segments. These can be on the same layer, but may also be broadside coupled from the adjacent layer. It is for this reason that orthogonal routing is recommended on adjacent layers (between planes) to minimize the coupling area.

Flight times of the critical signals are then examined. One could compare the matched lengths of each signal, but delay will vary depending on the meander pattern.

Since all products must comply with strict electromagnetic compliancy (EMC) regulations, all critical high-speed signals should be simulated to determine the amount of expected radiation.

Board-level simulation is engaged too often toward the end of the design cycle. Simulation should be done throughout the entire design process to ensure that the design is on track. A simulation service such as that provided by In-Circuit Design can complement your design team. It will save you time, money and frustration, but more importantly, from an engineer's or designer's point of view, give you confidence in the performance and reliability of the product. **PCB**

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## AT&S Leads Hermes Consortium

Miniaturization combined with ever increasing functionality and enhanced reliability has become part of our way of life, not least in the smartphone sector. The Hermes Consortium's task is to industrialize new miniaturization technologies.

In spring 2008 AT&S brought together eleven renowned European global players in one of the largest ever EU-sponsored projects. The participants came from different stages in the value chain in the automotive, aeronautical and other industrial sectors.

Hermes goes far beyond what is currently possible in connectivity. Series production processes are used to embed active components such as chips, as well as passive components such as resistors and capacitors in the interior of the PCBs. This creates additional space on the circuit boards, and the im-

provements in connectivity increase energy efficiency and extend the product's useful life.

One of the Consortium's main goals is to set standards for the industry, and to generate advantages over the competition in Asia. Industrial implementation of this technology opens up a wide range of potential applications in medicine (including new generations of hearing aids and pacemakers) and in functional modules for GPS, WLAN, Bluetooth and cameras. At the same time, AT&S is strengthening its position with existing customers as an innovation and technology leader, and is well placed to offer new solutions.

ECP technology has been brought to market in the course of the project following the successful construction of the production line in Hinterberg. AT&S picked up the Fast Forward Award 2011 for its ECP® technology. In the next few years, the complexity inside and on the surface of the modules will continue to grow, and the 3D capabilities of embedding technologies will pave the way for the next generation of mobile electronic devices.