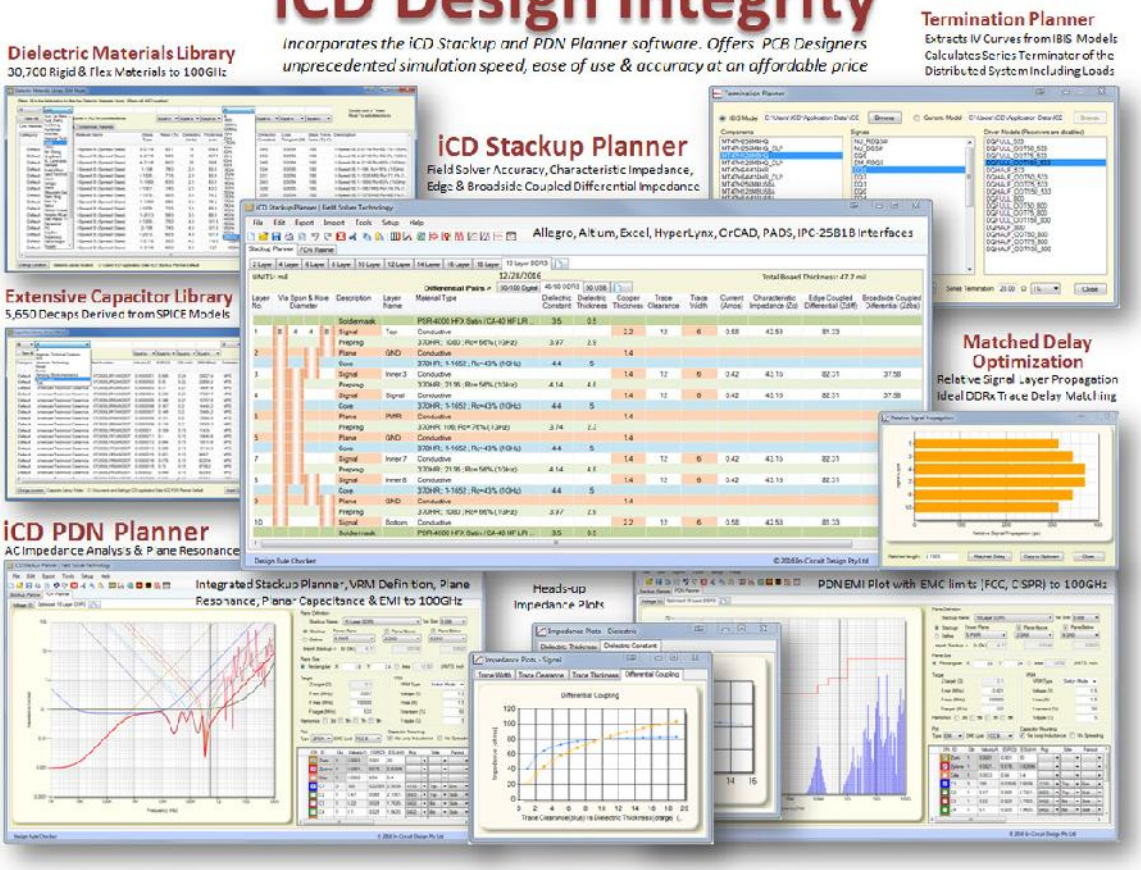
iCD Design Integrity

Incorporates the iCD Stackup and PDN Planner software. Offers PCB Designers unprecedented simulation speed, ease of use & accuracy at an affordable price



iCD Stackup Planner - Offers Engineers & PCB Designers unprecedented simulation speed, ease of use and accuracy at an affordable price

- Industry Leading 2D (BEM) Field Solver precision
- Characteristic impedance, edge-coupled & broadside-coupled differentiall impedance
- Relative Signal Propagation with 'Matched Delay Optimization'–ideal for DDRx design
- Termination Planner - series termination based on IBIS models & distributed system
- Unique Field Solver computation of multiple differential technologies per signal layer
- Extensive Dielectric Materials Library –over 30,700 rigid & flexible materials up to 100GHz
- Interfaces–Allegro, Altium, Excel, HyperLynx, OrCAD, PADS, Zmetrix TDR, Zuken & PC-2581B

iCD PDN Planner - Analyze multiple power supplies to maintain low AC impedance over entire frequency range dramatically improving product performance

- Fast AC impedance analysis with plane resonance and projected EMI
- Definition of plane size, dielectric constant & plane separation
- Extraction of plane data from the integrated iCD Stackup Planner
- Definition of voltage regulator, bypass/decoupling capacitors, mounting loop inductance
- PDN EMI Plot with FCC, CISPR & VCCI Limits. Frequency range up to 100GHz
- Extensive Capacitor Library –over 5,650 capacitors derived from SPICE models

"iCD Design Integrity software features a myriad of functionality specifically developed for high-speed design."
- Barry Olney

In-Circuit Design Pty Ltd

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New Functionality Improves Designer's Productivity

by Barry Olney
IN-CIRCUIT DESIGN PTY LTD / AUSTRALIA

Productivity features not only save time-to-market, but they also curb frustration. One of the most common issues that managers and PCB designers face today is lack of time. Unlike money, time is a non-renewable resource. Once time has passed, it is gone forever. With that said, getting more work done, in the same period of time, by using the right tools results in higher profits. Add it all up and it equates to cost savings and improved productivity. Integrated software is the key to efficient PCB design.

One of the main details lacking in today's PCB design software is the flow of impedance control from design capture through to board fabrication. If the impedance of all the required technologies, used in the design, is determined up-front at the time of capture, the engineer's intent should be preserved and flow through to downstream tools. However, that scenario rarely happens. Many PCB designers simply select the trace width and spacing, that they typically use assuming all FR-4 is the same, and start routing, thinking that the fab shop can fix it later. This is due to their inability to define the requirements as they rely on their fab shop's feedback, on impedance control, after completion of the Gerbers. This is analogous to shutting the gate once the horse has bolted.

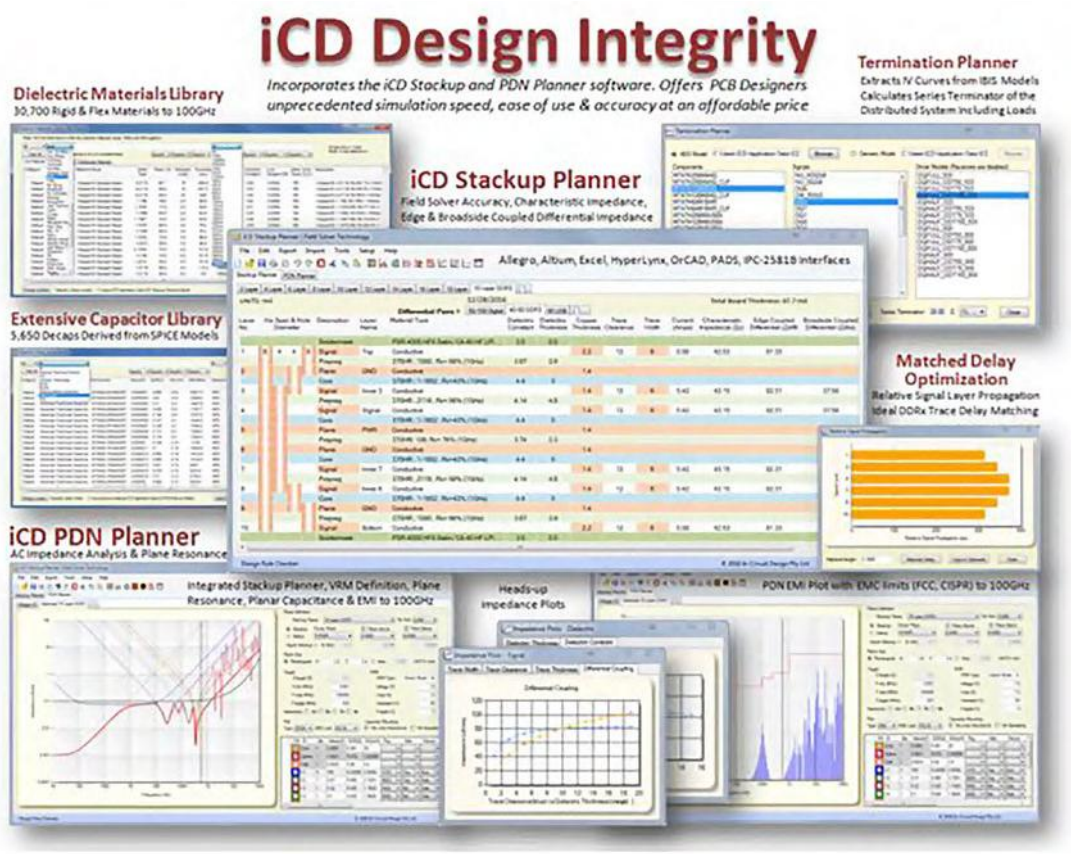

Figure 1: iCD Design Integrity productivity features.

I originally came up with the concept of an online impedance calculator way back in 1994 when I was working on the PCB layout and design for a new generation of SPARC 20 servers. We basically reformatted a Sun SPARC 20 pizza box motherboard to fit into a 5.25-inch drive slot. This was of course a tight exercise, but my idea was this: If I could physically fit all the required chips and connectors on the board, then it could be routed. This design required a 12-layer motherboard, and I used the IPC-317 "Design Guidelines for Electronic Packaging Utilizing High Speed Techniques" closed-loop equations to determine the signal layer impedance. The maximum CPU frequency was 200MHz, so there was plenty of margin.

To cut a long story short, after months of development, the project was completed and launched into the market. In 1995, the development team received an IEEE Engineering Excellence Award for the design. The server was subsequently licensed to a US company, jointly owned by Fujitsu and Sun Microsystems. Under license, the manufactured machine, a US-built SparcPlug Station, won the Best Performance category in the 1997 US AIM "Hot Iron" Awards.

During the development phase, as with all complex equations, I kept getting different results each time I manually calculated the impedance of a signal layer. Realizing that other designers have a similar problem, and a need to control the impedance of high-speed designs, we decided to write the code for an online impedance calculator based on the closed loop equations to simplify the process. This was first launched in 1995 and has developed, from its humble beginnings, into the iCD Stackup Planner, which today has very accurate field solver technology. Since then, we have had over 15,000 registered users globally. Of course, the product today has matured and is quite different from the original online tool, but our philosophy remains the same: a focus on simulation speed, ease of use and accuracy at an affordable price.

We have created a centralized, shared, impedance planning environment that connects materials, PDN analysis, stackup planning, signal integrity, PCB design and fabrication, consolidating the impedance control from schematic to fabrication. The impedance is planned pre-layout and flows through the design process to fabrication–achieving right first time design.

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Bi-directional Interfaces were developed for the most commonly used EDA tools: Allegro, Altium Designer, HyperLynx, OrCAD, PADS, and more recently the new IPC-2581B format. The IPC-2581B format interface has now been thoroughly tested by the IPC-2581 Consortium. This new feature gives the iCD Stackup Planner the ability to import/export Cadence Allegro and OrCAD stackups and to import Altium Designer, PADS Pro, Xpedition and Zuken CR-8000 stackups.

This allows the designer to either extract the stackup from their layout tool into the Stackup Planner or create a new stackup from scratch. Materials can then be inserted from the 30,700 available rigid and flex materials to greatly increase the accuracy of impedance, allowing for multiple differential pair technologies on the one substrate. The completed stackup is then exported back to the layout tool and design rules are automatically created to match the routing requirements. An Excel fabrication drawing can also be automatically created to inform the fabricator of the stackup and materials required single ended, edge and broadside coupled differential pairs and microvia spans.

The iCD Design Integrity suite of tools incorporates both the Stackup and PDN Planner, plus a myriad of new functionality specifically

developed for high-speed PCB design as shown in Figure 1. Over the past year, we have added the following productivity features:

- Relative signal propagation with Matched Delay Optimization feature
- Termination Planner—IV curves extracted from IBIS models
- Heads-up impedance plots created by multiple field solver passes
- PDN EMI Plot with FCC, CISPR and VCCI EMC limits
- IPC-2581B format, bi-directional interface
- Dielectric materials library of 30,700 rigid and flexible materials up to 100GHz.
- Capacitor library of 5,650, with Samsung caps added

Today's high-speed interfaces simply cannot be modeled using a match-to-length methodology—an approach that conventional PCB design tools support. This is because of the tight timing required. A matched length of 2.3 inches for a DDR3/4 data lane, for instance, can produce up to 70ps delta, between signal layers, leaving the timing way outside the required setup and hold times.

Consider, for example, a DDR3 interface with eight byte lanes. Each byte lane has data signals, strobe signals, and mask signals. And each grouping of signals has its own set of signals with eight signals in a byte. The timing within each byte lane must be within ~30ps for the highest speed memory.

Signals propagate at the speed of light in free space. However, this speed varies dramatically depending on the surrounding dielectric materials. Each layer of a multilayer PCB can have a very different propagation speed. This is particularly important for the latest high-speed DDR3/4 memory devices. The new Matched Delay Optimization feature of the iCD Stackup

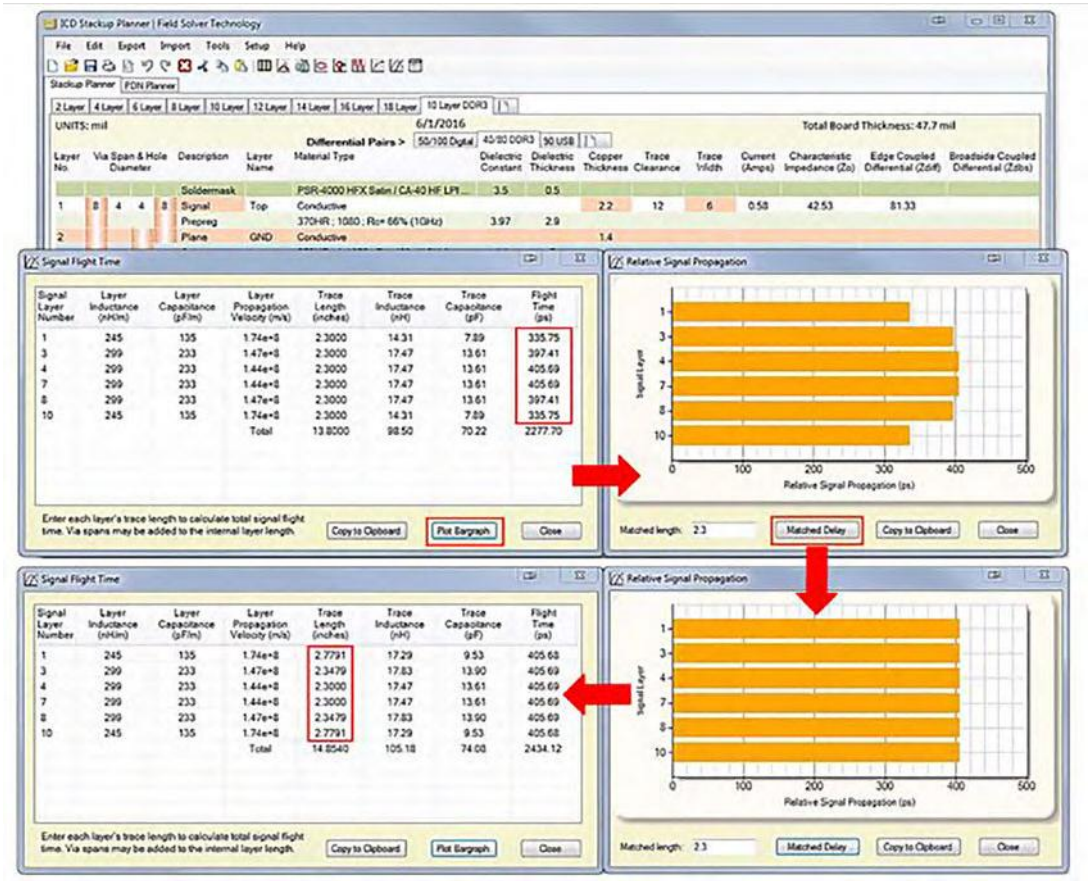


Figure 2: Matched delay optimization of each signal layer's relative flight time.

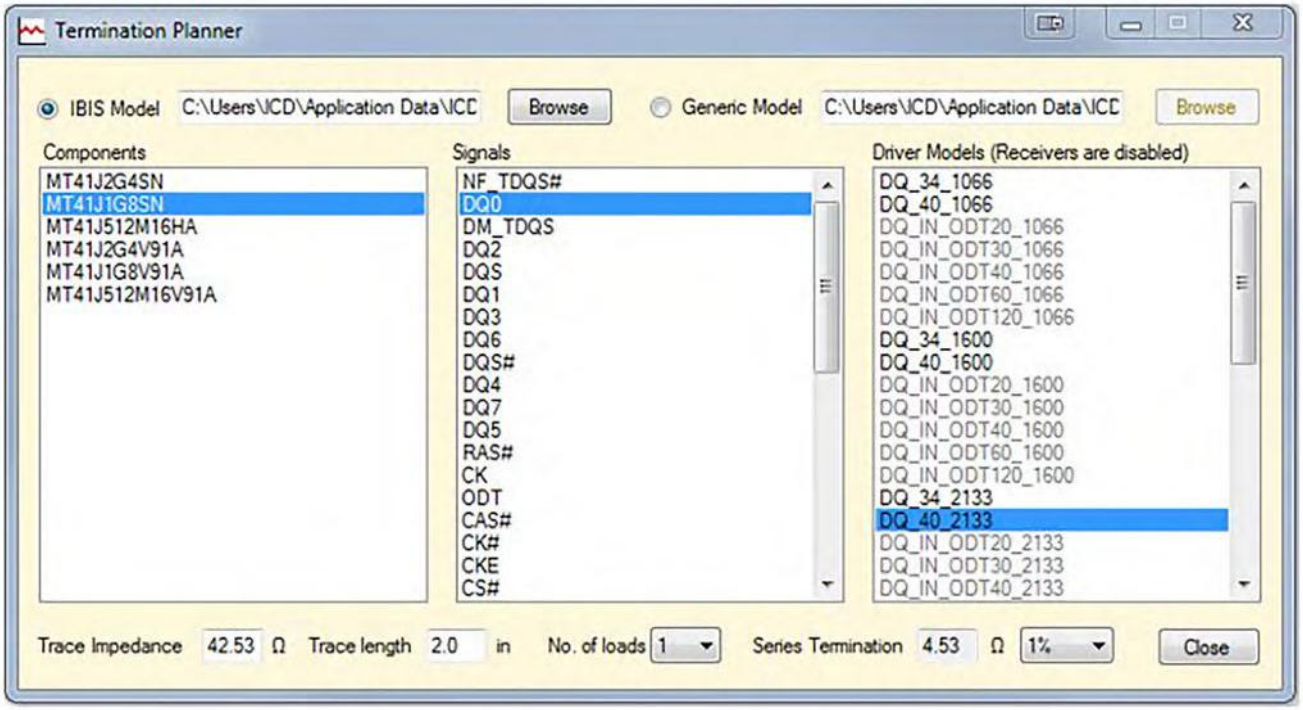


Figure 3: Matching a DDR3 driver IC to the transmission line.

Planner allows you to not only match the length of busses, but to take this one step further by automatically calculating the appropriate length required to match the delay exactly. The integrated field solver simulates the flight time, of each signal layer, to quickly give you the results you need to effectively route memory.

The relative signal propagation, of each signal layer, is displayed as a bar graph, once the matched length has been set (Figure 2). Selecting Matched Delay automatically optimizes the length, of each signal layer, to match the maximum delay. The users can then route the data lane to the exact delay, in their preferred design tool.

Also, it is one thing to perfectly match the delay of the transmission lines. But unfortunately, when using mainstream PCB layout software, one really has no idea what the driver impedance is, let alone the capability to match the driver to the impedance of the transmission line. The iCD Termination Planner addresses this issue.

Firstly, the attributes required to determine the source impedance of the driver, are extracted from an IBIS model IV curves. Then the required series termination resistance is calculated, based on a distributed system, to match the transmission line for the selected layer in the iCD Stackup Planner. If the IBIS model is not available (or produces an error) the user may use Generic Models to calculate an approximate series termination. Generic models include: typical DDRx, Display Port, ECL, HDMI, LVCMOS and LVTTL gates, Mini-LVDS, NAND Flash, PCI, SDRAM, HSTL and SSTL models.

The number of loads on the transmission line also has an effect on the required value of series termination; as the IC input inductance and capacitance tend to roll-off the signal rise time. This can be adjusted from 1–6 loads and automatically compensated for in the calculation.

Benefitting from 22 years of customer feedback and product development, the iCD Design Integrity software now provides numerous productivity tools for the high-speed PCB designer. The software was designed and built by PCB designers, specifically for PCB designers. We know what you need and what you want as we also do many real-world PCB designs and simulations ourselves. The tools are easy to use

and integrate with all the popular EDA tools to enhance your process efficiency. Beyond 2016, iCD will continue to develop new features to enable productivity gains as new methodologies and technologies arise. **PCBDESIGN**

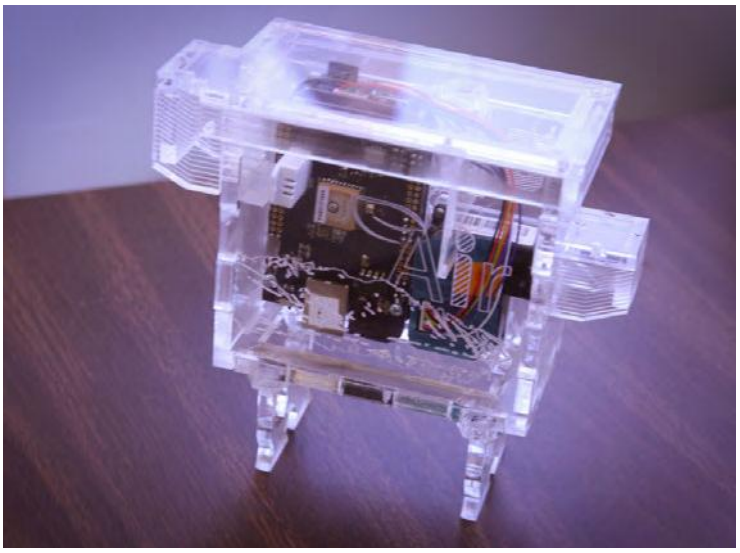
References

1. Barry Olney's Beyond Design column: Rock Steady Design.

2. A full list of manufacturers and materials available in the iCD Dielectric Materials Library is available here.

Barry Olney is managing director of In-Circuit Design Pty Ltd (ICD), Australia. This PCB design service bureau specializes in board-level simulation, and has developed the ICD Stackup Planner and ICD PDN Planner software. To read past columns, or to contact Olney, click here.

The Building Blocks for Bad Air



This season, assistant professor Kerry Kelly and associate professor (lecturer) Tony Butterfield have launched the AirU program for Salt Lake County high schools in which they visit science classrooms to talk about air quality and help students build a functional air pollution detector kit out of toy blocks and an inexpensive computer board. Beginning this month, the professors also will leave their own low-cost portable air-quality sensor with each classroom they visit so students can test and maintain them as well as collect data for researchers about pollution throughout the Salt Lake Valley.

"We started out with candy containers like Tic Tacs and other things and decided that wouldn't work," he says. "Then we realized [toy blocks] were the way to go because they [students] could build them into any shape they want."

So far, the team has built 15 kits. The professors use a small fog machine to demonstrate how the sensor works.

In addition to the toy-block sensors, Kelly, Butterfield and students from the University of Utah's electrical and computer engineering department also designed and created low-cost portable air pollution monitors that they will begin leaving in each classroom they visit. These monitors — about the size of a small box of tissues — are similarly powered by a low-cost computer board but are higher-grade than the toy-block monitors and have sensors that can specifically detect and measure particulate matter, temperature, humidity, carbon monoxide and nitrogen dioxide. They also are equipped with GPS and will be connected to the Internet wirelessly. The professors will ask the students to maintain the sensors and help test their reliability.

Ultimately, Butterfield and Kelly want to distribute as many as 50 of their research-grade sensors in schools around Salt Lake County to track pollution throughout the valley. They also want to eventually sell the kits for personal home use once they get the cost down.