



BOARD LEVEL SIMULATION SPECIALISTS

ICD Stackup Planner - offers engineers/PCB designers unprecedented simulation speed, ease of use and accuracy at an affordable price

- 2D (BEM) field solver precision
- Characteristic impedance, edge-coupled & broadside-coupled differential impedance
- Unique field solver computation of multiple differential technologies per stackup
- Heads-up impedance plots of signal and dielectric layers
- User defined dielectric materials library - over 16,250 materials up to 100GHz

ICD PDN Planner - analyze multiple power supplies to maintain low impedance over entire frequency range dramatically improving product performance

- Fast AC impedance analysis with plane resonance
- Definition of plane size/shape, dielectric constant & plane separation for each on-board power supply
- Extraction of plane data from the integrated Stackup Planner
- Definition of voltage regulator, bypass/decoupling capacitors, mounting loop inductance
- Frequency range up to 100GHz
- Extensive Capacitor Library – over 5,250 capacitors derived from SPICE models

Generic Multilayer Specifications for Rigid PCB's

1.1 GENERAL

1.1.1 This specification has been developed for the fabrication of rigid SMT and Mixed Technology Multilayer Printed Circuit Boards (PCB's) of less than 12 inches [300 mm] square.

1.1.2 Unless otherwise specified, the finished board shall meet:

- (a) Master 1X hole symbology plot.
- (b) Specific requirements of other sheets of this board drawing package.
- (c) In general, the latest revision of applicable standards of the Institute for Interconnecting and Packaging Electronic Circuits (IPC) i.e., IPC-6011/6012 Class III and IPC-2615.

1.1.3 In the event of a conflict in supplied drawings, the order of precedence that shall prevail is listed below:

- (a) Master drawing.
- (b) Specific deviation PCB specifications, if referenced on the Master drawing.
- (c) This generic specification.
- (d) Any relevant IPC documents referenced in the Generic PCB specifications.

1.1.4 A drill file defining plated hole and tooling hole diameter size(s) and locations has been supplied. The tooling holes shall be drilled in the initial drilling operation. If additional non-plated holes are required, a separate drill file may be supplied.

(a) The format of the files is EXCELLON.

- 2 whole unit digits.
- 4 digits of precision.
- No leading zero suppression.
- Repeat co-ordinate omission.
- Absolute data.
- Start of file "M72".
- End of file "M30".
- Units Mil.

(b) The information in the file has been sorted by hole diameter size.

(c) The information in the file has been optimised for minimising drill movement.

1.1.5 The board and any cut-outs shall be routed to the size specified on the PCB master drawing.

1.2 PHOTOGRAPHIC REPRODUCTION

1.2.1 If files have been supplied on digital format.

(a) The format of the files is Gerber.

2 whole unit digits.

4 digits of precision.

No leading zero suppression.

Repeat co-ordinate omission.

Absolute data.

Begin file string "M64".

End of file string "M02".

Units Mil.

(b) The relevant Aperture toolset is supplied or appended to the 274X (Extended Gerber) file.

(c) The Gerber files may only be edited to panelise the layer plots, and to allow for etch factor.

1.2.2 If films have been supplied.

(a) Only the 1X master patterns supplied are to be used for photographic reproduction of the circuit patterns, soldermasks and silkscreen legends. No changes are to be made to the 1X master patterns without prior approval. The substitution of prints or other copies of the 1X master patterns is not acceptable.

(b) The 1X master conductor patterns are supplied to the vendor on 7 mil [0.275 mm] thick Estar based film with a stabilised gelatin emulsion.

CONSTRUCTION

1.3.1 The following tables define the multilayer substrate of the completed printed wiring board. The artwork identification refers to the name of the layer as it appears on the master artwork pattern. Layer 1 is always the Primary side. The last layer is always the Secondary side.

The substrates were constructed on the ICD Stackup Planner (download from www.icd.com.au) The dielectric materials used are stocked by Select Circuits, Santa Ana, CA (www.selectcircuits.com) All units are in microns.

Table 1. 2 Layer

ICD Stackup Planner – www.icd.com.au								14/10/2010			
Layer		Material	Dielectric		Copper	Trace		Impedance	Edge Coupled	Broadside Coupled	Description
Number	Name	Type	Constant	Thickness	Thickness	Clearance	Width	Characteristic(Zo)	Differential(Zdiff)	Differential(Zdbs)	
1	Top	Liquid Photo Imageable	3.3	12.7							Soldermask
		Conductive			17	380	380	123.24	153.72		Signal
2	GND	FR408 (180 Tg)	3.7	1500							Core
		Conductive			35						Plane
		Liquid Photo Imageable	3.3	12.7							Soldermask

Table 2. 4 Layer

ICD Stackup Planner – www.icd.com.au 14/10/2010											
Layer Number	Material Name	Type	Dielectric		Copper Thickness	Trace Clearance	Width	Impedance Characteristic(Zo)	Edge Coupled Differential(Zdiff)	Broadside Coupled Differential(Zdbs)	Description
		Liquid Photo Imageable	3.3	12.7							Soldermask
1	Top	Conductive			17	300	300	61.91	106.95		Signal
		FR408 1080 (180 Tg)	3.7	63.5							Prepreg
		FR408 7628 (180 Tg)	3.7	165.1							Prepreg
2	GND	Conductive			335						Plane
		FR408 (180 Tg)	3.7	990							Core
3	VCC	Conductive			35						Plane
		FR408 1080 (180 Tg)	3.7	63.5							Prepreg
		FR408 7628 (180 Tg)	3.7	165.1							Prepreg
4	Bottom	Conductive			17	300	300	61.91	106.95		Signal
		Liquid Photo Imageable	3.3	12.7							Soldermask

Table 3. 6 Layer

ICD Stackup Planner – www.icd.com.au 14/10/2010											
Layer Number	Material Name	Type	Dielectric		Copper Thickness	Trace Clearance	Width	Impedance Characteristic(Zo)	Edge Coupled Differential(Zdiff)	Broadside Coupled Differential(Zdbs)	Description
		Liquid Photo Imageable	3.3	12.7							Soldermask
1	Top	Conductive			17	200	300	57.46	93.8		Signal
		FR408 106 (180 Tg)	3.7	43							Prepreg
		FR408 1080 (180 Tg)	3.7	58							Prepreg
		FR408 2116 (180 Tg)	3.7	99							Prepreg
2	GND	Conductive			35						Plane
		FR408 (180 Tg)	3.7	355							Core
3	Inner 3	Conductive			17	200	300	57.01	91.36	82.61	Signal
		FR408 2116 (180 Tg)	3.7	99							Prepreg
		FR408 2116 (180 Tg)	3.7	99							Prepreg
		FR408 2116 (180 Tg)	3.7	99							Prepreg
4	Inner 4	Conductive			17	200	300	57.01	91.36	82.61	Signal
		FR408 (180 Tg)	3.7	355							Core
5	VCC	Conductive			35						Plane
		FR408 106 (180 Tg)	3.7	43							Prepreg
		FR408 1080 (180 Tg)	3.7	58							Prepreg
		FR408 2116 (180 Tg)	3.7	99							Prepreg
6	Bottom	Conductive			17	200	300	57.46	93.8		Signal
		Liquid Photo Imageable	3.3	12.7							Soldermask

Table 4 8 Layer

ICD Stackup Planner – www.icd.com.au 14/10/2010											
Layer Number	Material Name	Type	Dielectric		Copper Thickness	Trace Clearance	Width	Impedance Characteristic(Zo)	Edge Coupled Differential(Zdiff)	Broadside Coupled Differential(Zdbs)	Description
		Liquid Photo Imageable	3.3	12.7							Soldermask
1	Top	Conductive			17	127	127	58.93	101.86		Signal
		FR408 2116 (180 Tg)	3.7	96.52							Prepreg
2	GND	Conductive			35						Plane
		FR408 (180 Tg)	3.7	152.4							Core
3	Inner 3	Conductive			17	127	127	49.8	87.93		Signal
		FR408 2113 (180 Tg)	3.7	73.66							Prepreg
		FR408 2116 (180 Tg)	3.7	96.52							Prepreg
4	VDD	Conductive			35						Plane
		FR408 (180 Tg)	3.7	533.4							Core
5	GND	Conductive			35						Plane
		FR408 2116 (180 Tg)	3.7	96.52							Prepreg
		FR408 2113 (180 Tg)	3.7	73.66							Prepreg
6	Inner 6	Conductive			17	127	127	49.8	87.93		Signal
		FR408 (180 Tg)	3.7	152.4							Core
7	VCC	Conductive			35						Plane
		FR408 2116 (180 Tg)	3.7	96.52							Prepreg
8	Bottom	Conductive			17	127	127	58.93	101.86		Signal
		Liquid Photo Imageable	3.3	12.7							Soldermask

Table 6 10 layer

ICD Stackup Planner – www.icd.com.au							14/10/2010				
Layer		Material	Dielectric		Copper	Trace		Impedance	Edge Coupled	Broadside Coupled	Description
Number	Name	Type	Constant	Thickness	Thickness	Clearance	Width	Characteristic(Zo)	Differential(Zdiff)	Differential(Zdbs)	
		Liquid Photo Imageable	3.3	12.7							Soldermask
1	Top	Conductive			35	180	100	53.72	102.5		Signal
2	GND	FR408 2113 (180 Tg)	3.7	73.66							Prepreg
		Conductive			35						Plane
		FR408 (180 Tg)	3.7	127							Core
3	Inner 3	Conductive			35	180	100	55.02	98.05	80.67	Signal
		FR408 1080 (180 Tg)	3.7	63.5							Prepreg
		FR408 1080 (180 Tg)	3.7	63.5							Prepreg
4	Inner 4	Conductive			35	180	100	55.02	98.05	80.67	Signal
		FR408 (180 Tg)	3.7	127							Core
5	VDD	Conductive			35						Plane
		FR408 106 (180 Tg)	3.7	35.56							Prepreg
		FR408 1658 (180 Tg)	3.7	114.3							Prepreg
		FR408 7628 (180 Tg)	3.7	165.1							Prepreg
6	GND	Conductive			35						Plane
		FR408 (180 Tg)	3.7	127							Core
7	Inner 7	Conductive			35	180	100	55.02	98.05	80.67	Signal
		FR408 1080 (180 Tg)	3.7	63.5							Prepreg
		FR408 1080 (180 Tg)	3.7	63.5							Prepreg
8	Inner 8	Conductive			35	180	100	55.02	98.05	80.67	Signal
		FR408 (180 Tg)	3.7	127							Core
9	VCC	Conductive			35						Plane
		FR408 2113 (180 Tg)	3.7	73.66							Prepreg
10	Bottom	Conductive			35	180	100	53.72	102.5		Signal
		Liquid Photo Imageable	3.3	12.7							Soldermask

Table 7 12 Layer

ICD Stackup Planner – www.icd.com.au											14/10/2010	
Layer		Material	Dielectric		Copper	Trace		Impedance	Edge Coupled	Broadside Coupled	Description	
Number	Name	Type	Constant	Thickness	Thickness	Clearance	Width	Characteristic(Zo)	Differential(Zdiff)	Differential(Zdbs)		
		Liquid Photo Imageable	3.3	12.7							Soldermask	
1	Top	Conductive			17	100	100	56.89	98.95		Signal	
2	GND	Conductive			35						Plane	
		FR408 2113 (180 Tg)	3.7	127							Core	
3	Inner 3	Conductive			17	100	100	57.93	95.87	87.94	Signal	
		FR408 1080 (180 Tg)	3.7	63.5							Prepreg	
		FR408 1080 (180 Tg)	3.7	63.5							Prepreg	
4	Inner 4	Conductive			17	100	100	57.93	95.87	87.94	Signal	
		FR408 (180 Tg)	3.7	127							Core	
5	VDD	Conductive			35						Plane	
		FR408 1080 (180 Tg)	3.7	63.5							Prepreg	
		FR408 1080 (180 Tg)	3.7	63.5							Prepreg	
6	Inner 6	Conductive			17	100	100	57.93	95.87	87.94	Signal	
		FR408 (180 Tg)	3.7	127							Core	
7	Inner 7	Conductive			17	100	100	57.93	95.87	87.94	Signal	
		FR408 1080 (180 Tg)	3.7	63.5							Prepreg	
		FR408 1080 (180 Tg)	3.7	63.5							Prepreg	
8	GND	Conductive			35						Plane	
		FR408 (180 Tg)	3.7	127							Core	
9	Inner 9	Conductive			17	100	100	57.93	95.87	87.94	Signal	
		FR408 1080 (180 Tg)	3.7	63.5							Prepreg	
		FR408 1080 (180 Tg)	3.7	63.5							Prepreg	
10	Inner 10	Conductive			17	100	100	57.93	95.87	87.94	Signal	
		FR408 (180 Tg)	3.7	127							Core	
11	VCC	Conductive			35						Plane	
		FR408 2113 (180 Tg)	3.7	73.66							Prepreg	
12	Bottom	Conductive			17	100	100	56.89	98.95		Signal	
		Liquid Photo Imageable	3.3	12.7							Soldermask	

Table 8 14 layer

ICD Stackup Planner – www.icd.com.au 14/10/2010											
Layer Number	Material Name	Type	Dielectric		Copper Thickness	Trace Clearance	Trace Width	Impedance Characteristic(Zo)	Edge Coupled Differential(Zdiff)	Broadside Coupled Differential(Zdbs)	Description
1	Top	Liquid Photo Imageable	3.3	12.7							Soldermask
		Conductive			35	100	100	53.72	93.43		Signal
2	GND	FR408 2113 (180 Tg)	3.7	73.66	35						Prepreg
		FR408 (180 Tg)	3.7	127							Plane
3	Inner 3	Conductive			35	100	100	51.45	85.68	57.39	Core
		FR408 2113 (180 Tg)	3.7	73.66							Signal
4	Inner 4	Conductive			35	100	100	51.45	85.68	57.39	Prepreg
		FR408 (180 Tg)	3.7	127							Signal
5	VDD	Conductive			35						Core
		FR408 1080 (180 Tg)	3.7	63.5							Plane
		FR408 1658 (180 Tg)	3.7	114.3							Prepreg
6	Inner 6	Conductive			35	100	100	57.44	95.91		Prepreg
		FR408 (180 Tg)	3.7	177.8							Signal
7	VCC	Conductive			35						Core
		FR408 1080 (180 Tg)	3.7	63.5							Plane
		FR408 1080 (180 Tg)	3.7	63.5							Prepreg
8	GND	Conductive			35						Prepreg
		FR408 (180 Tg)	3.7	177.8							Plane
9	Inner 9	Conductive			35	100	100	57.44	95.91		Core
		FR408 1080 (180 Tg)	3.7	63.5							Signal
		FR408 1658 (180 Tg)	3.7	114.3							Prepreg
10	VSS	Conductive			35						Prepreg
		FR408 (180 Tg)	3.7	127							Plane
11	Inner 11	Conductive			35	100	100	51.45	85.68	57.39	Core
		FR408 2113 (180 Tg)	3.7	73.66							Signal
12	Inner 12	Conductive			35	100	100	51.45	85.68	57.39	Prepreg
		FR408 (180 Tg)	3.7	127							Signal
13	VCC	Conductive			35						Core
		FR408 2113 (180 Tg)	3.7	73.66							Plane
14	Bottom	Conductive			35	100	100	53.72	93.43		Prepreg
		Liquid Photo Imageable	3.3	12.7							Signal
											Soldermask

Table 9 16 layer

ICD Stackup Planner – www.icd.com.au 14/10/2010											
Layer Number	Material Name	Type	Dielectric		Copper Thickness	Trace Clearance	Trace Width	Impedance Characteristic(Zo)	Edge Coupled Differential(Zdiff)	Broadside Coupled Differential(Zdbs)	Description
1	Top	Liquid Photo Imageable	3.3	12.7							Soldermask
		Conductive			17	100	100	56.89	98.95		Signal
2	GND	FR408 2113 (180 Tg)	3.7	73.66	35						Prepreg
		FR408 (180 Tg)	3.7	127							Plane
3	Inner 3	Conductive			17	100	100	54.07	91.3	64.66	Core
		FR408 2113 (180 Tg)	3.7	73.66							Signal
4	Inner 4	Conductive			17	100	100	54.07	91.3	64.66	Prepreg
		FR408 (180 Tg)	3.7	127							Signal
5	VDD	Conductive			35						Core
		FR408 1080 (180 Tg)	3.7	63.5							Plane
		FR408 1080 (180 Tg)	3.7	63.5							Prepreg
6	Inner 6	Conductive			17	100	100	54.26	91.53	66.11	Prepreg
		FR408 (180 Tg)	3.7	76.2							Signal
7	Inner 7	Conductive			17	100	100	54.26	91.53	66.11	Core
		FR408 1080 (180 Tg)	3.7	63.5							Signal
		FR408 1080 (180 Tg)	3.7	63.5							Prepreg
8	VCC	Conductive			35						Prepreg
		FR408 (180 Tg)	3.7	127							Plane
9	GND	Conductive			35						Core
		FR408 1080 (180 Tg)	3.7	63.5							Plane
		FR408 1080 (180 Tg)	3.7	63.5							Prepreg
10	Inner 10	Conductive			17	100	100	54.26	91.53	66.11	Prepreg
		Dielectric	4.3	76.2							Signal
11	Inner 11	Conductive			17	100	100	54.26	91.53	66.11	Core
		FR408 1080 (180 Tg)	3.7	63.5							Signal
		FR408 1080 (180 Tg)	3.7	63.5							Prepreg
12	VSS	Conductive			35						Prepreg
		FR408 (180 Tg)	3.7	127							Plane
13	Inner 13	Conductive			17	100	100	54.07	91.3	64.66	Core
		FR408 2113 (180 Tg)	3.7	73.66							Signal
14	Inner 14	Conductive			17	100	100	54.07	91.3	64.66	Prepreg
		FR408 (180 Tg)	3.7	127							Signal
15	VCC	Conductive			35						Core
		FR408 2113 (180 Tg)	3.7	73.66							Plane
16	Bottom	Conductive			17	100	100	56.89	98.95		Prepreg
		Liquid Photo Imageable	3.3	12.7							Signal
											Soldermask

*** Note: Layer separation figures and materials are a guide only. They may be altered to meet the minimum characteristic impedance specified in section 7.**

1.3.2 The total copper to copper thickness of the multilayer printed wiring board shall be 0.062" \pm 0.007" [1.574mm \pm 0.178mm].

1.3.3 Layer identification is included on each master artwork pattern within the printed wiring board circuit area. This is a precisely located and configured identification that is used to assure that the layers have been laminated in the correct order and orientation. When correctly superimposed on one another after the laminating process, the first half of the layers should be readable from the primary side, while the second half should be readable from the secondary side. (On older artworks only the secondary side layer may be reverse reading).

1.4 MATERIAL

- 1.4.1 (a) Base material: FR408 (FR406 can be used if not a HSD PCB)
(b) Base Colour: NATURAL

1.4.2 The laminate copper foil weight for the signal layers is a recommendation only. It is the vendor's responsibility to select the correct laminate foil thickness to meet the requirements of this specification (such as final copper thickness, hole plating, conductor width tolerance, etc.).

1.5 UL IDENTIFICATION

1.5.1 The circuit board Manufacturer's marking, certifying Underwriter's Laboratories (UL) recognition of the process (minimum 94V-0) is to be located on the secondary side of the board, in close proximity to the PCB Artwork number.

1.5.2 The marking shall consist of either the Manufacturer's logo followed by full classification designation, such as 94V-0, or the Manufacturer's logo followed by a type designation.

1.5.3 When there is more than one factory, the factory designation shall be included.

1.6 INNER LAYER SURFACE TREATMENT

1.6.1 A heavy oxide (ie. black or brown oxide) surface treatment is required to increase copper surface area and promote lamination bond strength.

1.7 CONDUCTORS

1.7.1 The minimum characteristic impedance of the signals layers shall not be less than 70 ohms. The artwork may be modified to achieve this.

The narrowest copper conductor width and spacing on the signal layers is:

(a) **Width: 0.004"** [0.100mm] nominal.

(b) **Spacing: 0.004"** [0.100mm] nominal.

(Note that the artwork is 1:1, no etch factor or characteristic impedance allowance has been made.)

1.7.2 The minimum spacing shall not be less than 80% of nominal spacing.

1.7.3 No defect shall reduce the cross section of a copper conductor by more than 20%.

1.7.4 No damaged or broken copper conductor may be repaired without prior approval.

1.8 HOLE AND CONDUCTOR PATTERN REGISTRATION

1.8.1 Hole location tolerances are grade C ($\pm 0.003"$ [0.0762mm])

1.8.2 The layer-to-layer registration between any two layers shall be within 0.002" [0.0508mm].

1.8.3 The minimum annular ring on all land areas on the signal layers shall not be less than grade C (0.002" [0.0508mm]). The thickness of the metal in the plated-through-hole is included. The minimum annular ring should be not less than the maximum etch back allowance.

1.8.4 All features should be within 0.003" [0.076mm] of the position on the photo master.

1.9 SMEAR REMOVAL (Hole Cleaning)

1.9.1 The holes in the board shall be mechanically or chemically cleaned for the lateral removal of material from the internal layers prior to plating.

1.9.2 After plating, there shall be no evidence of resin smear or epoxy residue.

1.9.3 After plating, there shall be a direct bond of the plated copper to the foil copper of the internal layers. A line of demarcation is acceptable.

1.9.4 Etch back (removal of epoxy smear and glass fibres) is not required but acceptable.

1.10 PLATING (External Layers Only)

1.10.1 Plated-through-holes.

(a) Material: Copper.

(b) Thickness (on walls): 0.001" [0.0254mm] minimum.

(c) All holes shall be within the size tolerance after all plating and reflow operations have been completed.

1.10.2 Conductor paths other than printed edge board contacts (fingers):

(a) Copper: final copper thickness (base foil plus plating to be): 0.0015" [0.0381mm] minimum.

(b) Additional plating:

1. Material: RoHS compliant lead free HASL, Immersion Tin/Ag/Gold or electroless nickel.
2. Thickness: 0.0003" [0.00762mm] minimum at crown, after reflow.
3. For SMT boards the maximum bump height shall be 0.0015" [0.0038mm].

1.10.3 Contact Finger Plating.

(a) Material : Nickel/Gold 0.0001" [0.0025mm] minimum, low stress Nickel under 0.0001" [0.0025mm] minimum 99.7% pure gold, having a hardness of Knopp 140-220.

(b) Plating length from the leading edge of finger : 0.300" [7.72mm] minimum.

(c) The leading edge of the contact fingers are to be bevelled 0.020" \pm 0.010" [0.508mm \pm 0.254mm] by 45 degrees on both sides of the board.

1.11 SOLDERMASK

1.11.1 Soldermask on both sides over bare copper.

1.11.2 The soldermask 1X master patterns shall be used.

1.11.3 Mask with liquid photo imageable film. For SMT boards the soldermask shall be below the level of the pads.

1.11.4 The mask shall conform to the board's pad area size and configuration and shall not extend onto the pad area or fiducial marks. If the mask extends onto the pad area of via holes, the via holes shall be tented or plugged. The via hole diameters may be adjusted to achieve this.

1.11.5 Soldermask material is to be applied as specified by the material manufacturers.

1.11.6 Damaged or missing soldermask may not be repaired without prior approval.

1.11.7 Minimum soldermask thickness 0.001" [0.025mm].

1.12 SILKSCREEN LEGENDS

1.12.1 Silkscreen legends on Primary and Secondary side if supplied.

1.12.2 The silkscreen legends 1X master patterns shall be used.

1.12.3 Silkscreen shall be applied after application of solder mask.

1.12.4 The silkscreen ink shall not extend into any plated-through-hole, surface mount pad or secondary side through-hole pad.

1.12.5 The silkscreen ink shall be white.

1.12.6 The silkscreen legends shall be within 0.010" [0.0254mm] of the position on the photo master.

1.13 TEST COUPONS (IF PRESENT)

1.13.1 The coupon identification boxes are labelled to indicate the PCB Artwork / Revision numbers and shall be stamped to aid traceability.

1.13.2 The solder mask adhesion coupon shall be coated with soldermask, all other coupons shall be uncoated.

1.14 SOLDERABILITY

Test per IPC-S-804.

1.15 CRACKS, CHIPS AND BURRS

1.15.1 No cracks are allowed:

1.15.2 No chips, cracks or haloing about the periphery of the board shall extend onto the top or bottom face area of the board further than 0.030 inch [0.762mm] from the board edge.

1.15.3 The board edge shall be free from burrs and/or strands.

1.15.4 Visual cracks, chips, fibres and haloing from the inside edges of slots, notches, cut-outs or holes shall not exceed 0.005 inch [0.127mm] and shall be free from stray glass strands.

1.16 BOW OR TWIST

The Bow and Twist of the finished board shall be 0.5%. Actual values for bow shall be obtained using IPC-TM-650, section 2.4.22, 5.1 procedure No. 1.

Actual values for twist shall be obtained using IPC-TM-650, section 2.4.22, 5.2 procedure No. 2.

(For example, a PCB of 9.185" x 11.02" will have a maximum bow (R1-R2) of 0.055" [1.397mm] on its longest edge, and a twist (R1-R2) of 0.143" [3.63mm]).

1.17 DIELECTRIC WITHSTANDING VOLTAGE TEST

The dielectric withstanding voltage shall be applied between conductor patterns of each layer and the electrically isolated pattern of each adjacent layer. The dielectric withstanding voltage shall be per IPC-6012B class III. (1 KV DC for 30 seconds duration).

1.18 ELECTRICAL BARE-BOARD TESTING

All boards are to be 100% electrically tested for shorts and opens, but probing of vias is not required.

The copper feature to feature test voltage should be a minimum of 30V @ 40mA.

The board connectivity is to be verified from either the supplied netlist or a netlist extracted from the supplied Gerber files. "Golden-board" comparison is inadequate.

1.19 DOCUMENTARY EVIDENCE

Documentary evidence of all tests is to be provided.

1.20 PACKAGING

The finished boards shall be individually packed in unsealed thermoplastic bags containing no silicones or sulphur-containing material which might degrade solderability.

1.21 REFERENCES

IPC-2220	Series of Design Documents
IPC-2221	Generic Standard on Printed Board Design
IPC-2222	Sectional Standard on Rigid PWB Design
IPC-2223	Sectional Design Standard for Flexible Printed Boards
IPC-2224	Sectional Standard for Design of PWB's for PC Cards
IPC-2225	Sectional Standard for Organic Multichip Modules and Assemblies
IPC-2251	Design Guide for Electronic Packaging Utilizing High Speed Techniques
IPC-2615	Printed Board Dimensions and Tolerances
IPC-6011	Generic Performance Specification for Printed Boards
IPC-6012B	Qualification and Performance Specification for Rigid Printed Boards
IPC-7351	Generic Requirements for Surface Mount Design and Land Pattern Standard
IPC-TM-650	Test Methods Manual.
IPC-S-804	Solderability Test Methods for Printed Wiring Boards
IPC-SM-840D	Qualification and Performance of SolderMask for Printed Boards.

ICD Stackup Planner is used to construct the substrates and to calculate the required impedances. Download from www.icd.com.au