

Differential Pair Routing

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This application note discusses the selection and optimal settings of differential pair design rules

Basically, a differential pair is two complementary transmission lines that transfer equal and opposite signals down their length.

The debate rages as some argue that since the two halves of the pair carry equal and opposite signals a good ground connection is not required as the return current flows in the opposite signal. And, tight coupling between the signals is better than loose coupling as it reduces undesirable coupling from aggressor signals.

Others say that beyond the fact that differential pairs transfer equal and opposite signals, there are no special requirements that need to be considered when using differential pairs. They should be treated as two single ended signals. The signals of a differential pair don't need to be routed together, should not be tightly coupled and are not required to be routed to the differential impedance.

Hmm.... I am not getting into this argument as I look at PCB design from a practical Designer's point of view and the theory can be left to the experts to discuss.

However most agree on the advantages of differential signaling:

1. The ground (reference) connection between the driver and load can be poor and the signal quality will not be compromised.
2. The signal can be attenuated significantly (20 dB) and still function properly.
3. Because of the high noise immunity, they can carry extremely high data rates (10 Gb/s) compared to single ended transmission lines.
4. The equal and opposite nature of the differential pair means that demand on the power distribution network is less than for a similar single-ended data path.

So keeping both points of view in mind, I consider that symmetry is the key to successfully deploying differential signals in high speed designs. Maintaining the equal and opposite amplitude and timing relationship is the principle concept when using differential pairs.

Differential pairs also require matched length traces. For instance, DDR2 clocks need to be matched to within 25 MIL. This ensures that there is no skew between the signals of the pair and flight times will be identical which is an important factor.

To control crosstalk – keep aggressor signals as far away as possible from differential pairs especially in Microstrip (outer layers). A good rule of thumb here is: Clearance = 3 x trace width. Also reducing the signal layer to reference plane spacing (dielectric) improves crosstalk.

If the routing is dense then consider setting the clearance design rules to 2 x trace width to start with. There is a good feature in Altium Designer that I use frequently – the Parallel Segment Rule. This enables you to set a gap of 4 MIL (on the same layer or adjacent layer) for a maximum length of 500 MIL then the spacing must increase to 8 MIL.

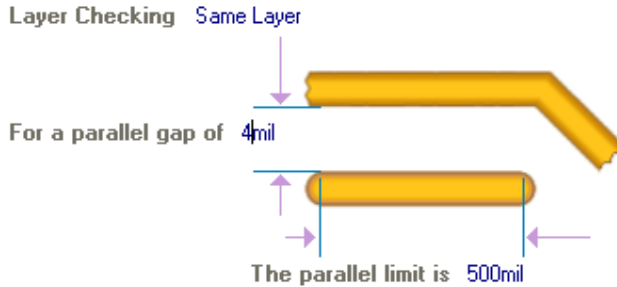


Fig. 1 Parallel Segment Rule

Also, placing copper pours next to one side of a pair isolates the two halves of the pair. This is another good reason not to pour copper ground planes on high speed digital designs. Keep ground pours well away from differential pairs. If you must have them use a clearance of 3 x trace width.

The amount of real estate available is also to be considered. Typically a DDR2 board will be routed with 4 MIL trace and 4 MIL clearance with vias 20 MIL pad and 8 MIL hole. This allows us to place the fanout vias under the BGA device and route out to open space. So generally, the 100 ohm differential clock will start at 4/4 (trace/clearance) and once clear of the BGA revert to 4/8.

Fig. 2 below shows a DDR2 clock routed differentially from the processor with a 4 MIL trace and 8 MIL spacing. The signals come out of the BGA, fanout within 200 MIL and drop to an internal signal layer to then be distributed to the memory chips.

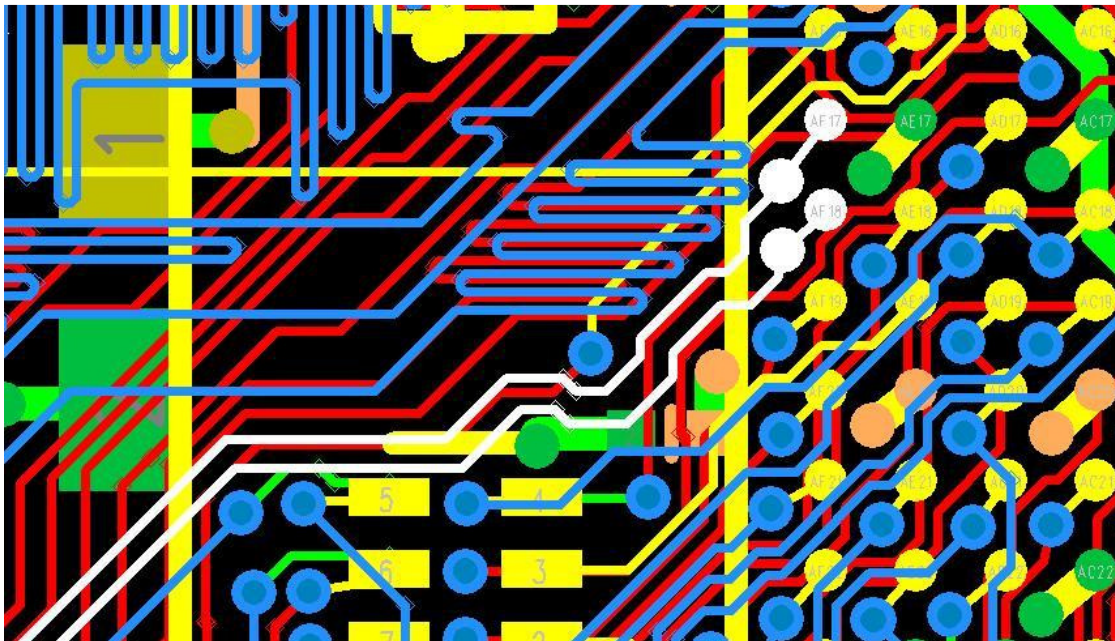


Fig. 2 DDR2 clock at 4 MIL trace 8 MIL spacing

In this case I was fortunate not to have an obstacle in the path of this pair. It is typical however to have to split the pair around a via, pin or other obstacle to get to the load. This is where tightly coupled pairs come unstuck. That is, the gap and hence differential impedance cannot be maintained and the result is a much higher impedance in the diverted area which creates reflections.

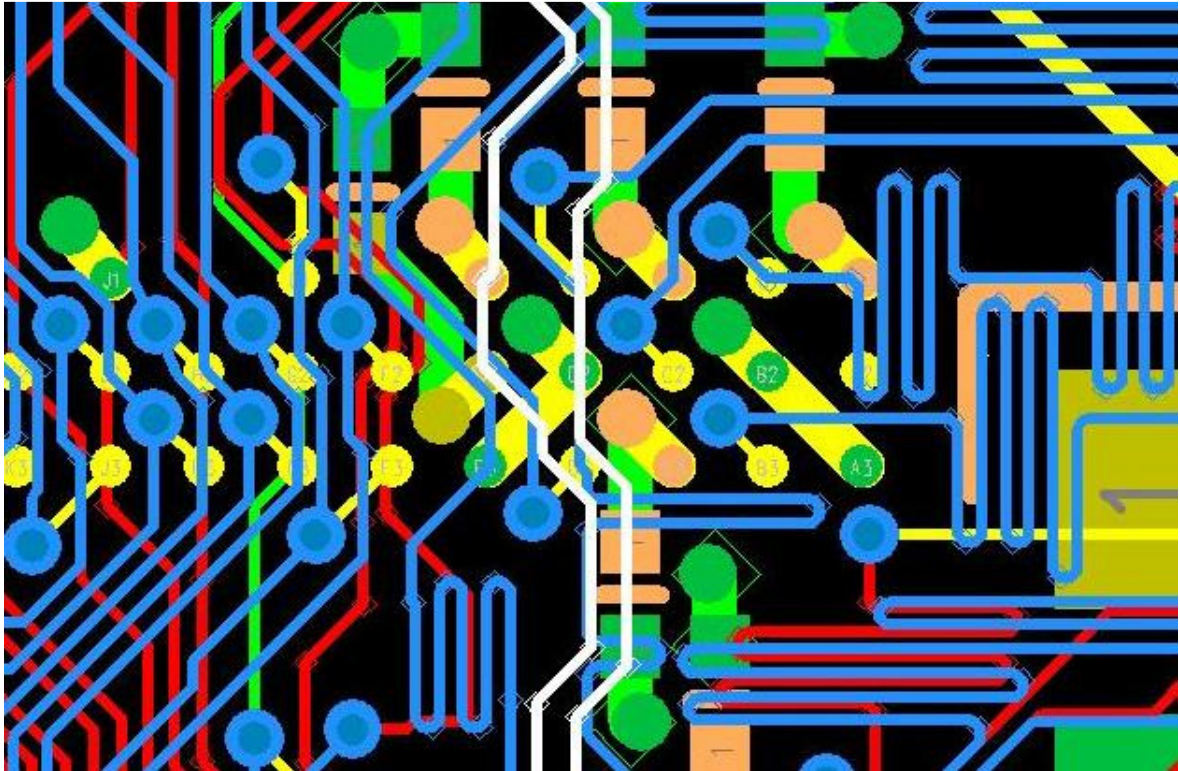


Fig. 3 shows how the gap increased from 8 MIL to 28 MIL around an obstacle then back to 8 MIL.

This brings us to another controversial point: whether to have close (tight) or loose coupling of the differential signals (where tight coupling is defined as 4/4; loose coupling is 4/12). Tight coupling is good for densely routed boards (aren't they all) but with tight coupling the clearance must be maintained along the entire length of the signal. As mention previously, this is not always possible because of the inevitable obstacle.

Leaving the theory of differential signaling aside – here's what works:

The rule of thumb Gap = 2 x trace width.

So for a 4 MIL trace a gap or clearance (edge to edge) should be in the order of 8 MIL. If we expand the 8 MIL gap to 28 MIL around an obstacle (e.g. 20 MIL via) the differential impedance increases by 3.85 ohms (3.85 %) but if we start with tight coupling of 4/4 and increase to 4/28 around an obstacle then the impedance does a massive jump of 25 ohms (25%). Clearly, this is way over the acceptable +/- 10% for controlled impedance boards (not considering the fabrication process variables).

Trace Width (MIL)	Clearance (MIL)	Zdiff (ohms)	% increase	
4	8	99.99		
4	28	103.84	3.85%	ideal
4	4	100.99		
4	28	126.79	25%	out of tolerance

ICD STACKUP PLANNER – www.icd.com.au 9/1/2011 Total Board Thickness: 61.8												
Differential Pairs > DDR2CLK USB SATA ETHERNET												
Layer	Material	Dielectric	Copper	Trace	Current	Impedance	Edge Coupled	Broadside Coupled	Description			
Number	Name	Type	Constant	Thickness	Thickness	Clearance	Width	(Amps)	Characteristic(Zo)	Differential(Zdiff)	Differential(Zdbs)	
1	Top	Conductive	3.3	0.5	1.4	8	4	0.31	53.53	99.99		Soldermask
		Dielectric	4.3	3								Signal
2	GND	Conductive			1.4							Prepreg
		Dielectric	4.3	10								Plane
3	Inner 3	Conductive			1.4	8	4	0.31	62.39	99.59		Signal
		Dielectric	4.3	10								Prepreg
4	VDD	Conductive			0.7							Plane
		Dielectric	4.3	6								Core
5	GND	Conductive			0.7							Plane
		Dielectric	4.3	10								Prepreg
6	Inner 6	Conductive			1.4	8	4	0.31	62.39	99.59		Signal
		Dielectric	4.3	10								Core
7	VCC	Conductive			1.4							Plane
		Dielectric	4.3	3								Prepreg
8	Bottom	Conductive			1.4	8	4	0.31	53.53	99.99		Signal
		Dielectric	3.3	0.5								Soldermask

Fig. 4 DDR2 clock differential pair of 100 ohms impedance

The above stackup was built with the ICD Stackup Planner (download from www.icd.com.au). The new HDI Designer Edition includes multiple differential pair definitions per layer.

These days it is quite common to have differential DDR2 clocks, USB pairs, PCI express pairs etc sharing the same layers on HDI boards. Until now the Designer had to calculate each impedance separately and somehow display the results meaningfully to fellow Designers and the PCB Fabricator. It is usually difficult enough to calculate one differential impedance but the Designer must now run both 100 ohm and 90 ohm impedances on the same layer.

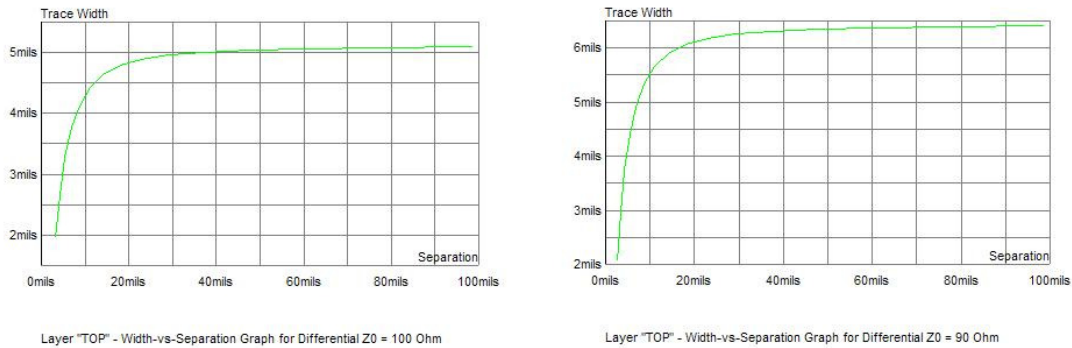


Fig. 5 Graph of trace width Vs clearance for 100 ohm and 90 ohm differential impedance

As previously mentioned, the 4/8 differential pair works well for 100 ohms differential impedance on this particular substrate. However, the 90 ohm USB signal would be best routed at 5.5/11 as any increase in trace separation will have minimal affect on impedance.

The new HDI Designer Edition of the ICD Stackup Planner addresses these issues. Simply select the desired number of layers 2 to 16 (or create your own unlimited layer stackup) and start inserting differential pairs. As you insert a new differential pair, the ICD Stackup Planner automatically calculates both the single ended (characteristic) and differential impedance of each layer. Simply adjust the variables to achieve the desired impedance of 100 or 90 ohms for a common substrate.

In conclusion:

1. Symmetry is the key to successfully deploying differential signals in high speed designs. Maintaining the equal and opposite amplitude and timing relationship is the principle concept when using differential pairs.
2. Match the length of each signal of the pair. This ensures that there is no skew between the signals of the pair and flight times will be identical.
3. Route the differential pairs to impedance and at the optimal spacing:
Gap = 2 x trace width
4. To control crosstalk – keep aggressors far away from differential pairs especially on Microstrip (outer layers).
A good rule of thumb here is: Gap = 3 x trace width.

References:

Advanced Design for SMT – Barry Olney
Design Techniques for DDR, DDR2 & DDR3 – Barry Olney
Embedded Signal Routing – Barry Olney
Copper Ground Pours – Barry Olney
Practical Differential Pair Design – Eric Bogatin
A treatment of Differential Signaling and its Design Requirements – Lee Ritchey
High Speed Digital Design – Howard Johnson
Routing Differential Pairs – Dennis Nagle, Cadence Design Systems
ICD Stackup Planner – download from www.icd.com.au

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