

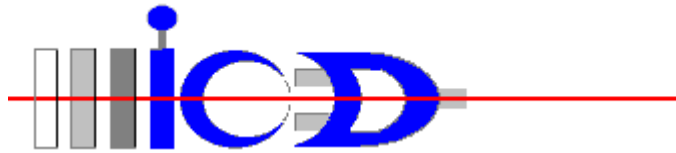
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ICD PDN Planner - analyze multiple power supplies to maintain low impedance over entire frequency range dramatically improving product performance

- Fast AC impedance analysis with plane resonance
- Definition of plane size/shape, dielectric constant & plane separation for each on-board power supply
- Extraction of plane data from the integrated Stackup Planner
- Definition of voltage regulator, bypass/decoupling capacitors, mounting loop inductance
- Frequency range up to 100GHz
- Extensive Capacitor Library – over 5,250 capacitors derived from SPICE models



The VeriBest Solutions Centre

EMC Design for High Speed PCB's - Barry Olney

Excessive emission of electromagnetic waves associated with transmitting switching signals and the susceptibility of circuits, within the high-speed digital system are forcing PCB designers to develop new design techniques.

In recognition of this, the Spectrum Management Agency (SMA) has introduced an electromagnetic compatibility (EMC) framework in Australia. The phase-in time frame proposed by the SMA is divided into four stages over two years, beginning January 1, 1996.

The Australian Electronics Development Centre (AEDC) regularly presents two courses: Advanced Design for Surface Mount Technology (SMT) and EMC - Solving the Problem in both Australia and New Zealand. These courses provide excellent background knowledge for both EMC design and compliancy.

Although the majority of EMC compliance issues are associated with equipment chassis shielding/grounding and cabling, PCB engineers and designers must pay attention to transmission line effects in high speed designs.

For example, the inherent timing requirements of a design will dictate the use of different device families. Wherever possible, these logic families should be confined geographically. Multiple pin grounds or controlled impedance connectors may mean less routing real estate or higher component costs, but may also be the differentiating factor between a functional and non-functional product. The transmission line geometry and multilayer stack-up construction are critical factors. Impedance matching, clock skewing, crosstalk, parallelism and power distribution all affect signal integrity. And, though, there are EDA tools on the market that can help control these problems, it's best to be familiar with the cause and effects of electromagnetic interference and compatibility and how to maintain control of a design.

Radiation and Antenna

At high frequencies, traces on a PCB act as a mono-pole or loop antennas. Differential-mode radiation is the electromagnetic radiation caused by currents consisting of harmonic frequency components flowing in a loop in the PCB. The radiation is proportional to the current loop area and the square of the frequency of the signal. Common-mode radiation is the electromagnetic radiation caused by current flowing in an unterminated trace (or terminated with a high input impedance device) and may require load terminating resistors to eliminate reflections. The radiation resembles that of a mono-pole antenna and the magnitude is proportional to the current per line length and frequency.

Unfortunately, the high frequency components of the fundamental (lowest frequency in a complex wave) radiate more readily because their shorter wavelengths are comparable to trace lengths, which act as antennas. Consequently, although the amplitude of the harmonic frequency components decreases as the frequency increases, the radiated frequency varies depending on the antennas/traces characteristics. For example, interference signals produced by computing devices tend to lie in the 10 to 300 MHz region.

At what speed should there be concern about wave propagation rather than just current in conductors? The rule is that transmission line effects become an important design consideration when the trace length approaches 1/7 of the wave-length of the signal being transported. If the system clock frequency is 300 MHz, the wavelength in FR4 is about 0.5 m.

Clock Speed or Rise/Fall Time?

Generally, the system clock is a repetition rate of a square wave pulse, and the pulse information of "1" or "0" is carried on the leading edge of the pulse. This edge must be permitted to rise or fall as quickly as possible. Frequency and the rise time of the signal are related by the relation:

$$Tr \text{ (rise time in nS)} = 0.35 / \text{frequency in GHz}$$

Table 1 shows the rise times and wavelengths for common high-speed IC's.

Device rise times & wavelengths				
	TTL	Schottky TTL	ECL	GaAs
Output Rise Time (ns)	6-9	2-3	0.45-0.75	0.05-0.20
Wavelength in free space (m)	6.8	2.5	0.52	0.086
Wavelength in FR4 (m)	3.1	1.2	0.24	0.04

e.g. for ECL: frequency = $0.35 / 0.45 = 777$ MHz

This translates to a wavelength of about 375 mm in free air or 175 mm in FR4 and 100 mm in ceramic. Therefore, if the trace length is more than 25 mm for PCB's fabricated from FR4, then the electromagnetic properties of the ECL signal and the transmission line effects should be considered.

Therefore, the signal rise/fall time, instead of the signal clock frequency, determines the critical signal speed. A steep rise/fall time may be slowed by loading the signal line with a damping/backmatching resistor close to the source.

Characteristic Impedance

Fifty to eighty ohm characteristic impedance is often used in high-speed designs. Lower impedance values cause excessive dI/dt crosstalk and can double the power consumed to create a heat dissipation problem. Higher impedances not only produce high crosstalk, but also produce circuits with greater EMI sensitivity and emission.

Table 2 illustrates the effect that physical properties have on the impedance (Z_0) of a transmission line.

Effects of physical properties on impedance	
Variable	Impedance
Increase trace width	Lower
Increase proximity of traces	Higher
Increase signal/plane spacing	Higher
Increase dielectric constant	Lower

The fields emanating from the surface of a conventional single/double-sided board are not guided by a controlled return conductor (i.e. reference plane). Rather, the fields tend to terminate on adjacent traces, which creates crosstalk. Some of these fields escape the surface of the PCB totally and radiate outward.

However, multilayer PCB's have ground and power distribution conductors embedded as planes in the substrate. The return currents for the signal traces flow through the reference plane, which is in close proximity to the trace. Also, the use of planes provides the low impedance power distribution necessary for good supply decoupling.

Enclosing signal traces between the ground and power planes provides a shield which reduces both radiation (by up to 45 dB) and susceptibility to radiation, as well as providing ESD protection. It is good practice to route high speed, fast rise time signals between these planes to eliminate radiation. If a large capacitance exists between the rails, both ground and power planes may be used as reference planes.

Recent studies, conducted by Hewlett Packard have found that there is up to 20 dB greater emissions from edge-located traces compared to traces located in the centre of the board on outer layers. Yet, the same test performed on buried traces indicated no change as the traces were placed nearer the PCB edges.

Recently, software has become available that can be used to calculate the impedance and the velocity of propagation of each layer for a given trace width. For reduced crosstalk, alternate layers should be rotated by 90 degrees (e.g. layer one = horizontal, layer three = vertical, layer four = horizontal, etc).

Generating Noise

Clock circuits have the highest toggle rates of all circuits and are the primary source of noise generated in digital circuits. Clock timing and skew are critical factors affecting circuit performance. It is best to centrally locate the clock generator and distribute it radially. Radiated fields from the outward flowing currents tend to cancel, which reduces and synchronises propagation delays throughout the board. Equal mark-to-space ratios with controlled rise/fall times also help reduce noise by removing even harmonics.

In high-speed systems, the clock cycle time is usually shorter than the propagation delay for a signal to travel from one device to another. For the system to perform correctly at high speeds, a well-controlled propagation time is required, and adjustments in the timing skew for some signals may be necessary. Tuned delay can be achieved with the aid of software.

Alternatively, trace lengths can be equalised manually to avoid skew by using a star routing pattern from the source.

Component Density = Trace Density = Crosstalk

Generally, an assembly is populated as densely as possible with SMDs to minimise the size of the board and reduce propagation time. The result is, of course, that traces must run close to each other, which creates crosstalk. Crosstalk is the transfer of pulse energy by the electromagnetic field from a source line to a victim line. The intensity of the coupled signal decreases with shorter adjacent line segments, wider line separations, lower line impedance and longer pulse rise times.

Field solver software is recommended to predict transmission line characteristic impedances, propagation velocities and crosstalk. As clock speeds increase, this may become mandatory. To accurately estimate delays and crosstalk, a layer stackup must be coupled with the field solver. The result is a quick and accurate characterisation of the layout traces that is dynamically updated on the fly. Note that the dielectric constant of FR4 material can vary by as much as 20%.

Logic Families Don't Mix

Mixing logic families is not advised because of their differences in voltage swings, noise margins and logic levels. For example, Schottky TTL swings 3 V while the ECL family has only 100 mV DC noise margin. Mixing these two logic families could cause significant undesired coupling.

For high-speed devices, switching activity is accompanied by equally high-speed demands for changes in current from the power supply. If several devices are switching at the same instant, the power distribution system must be able to supply the current while maintaining the supply voltage within the specified limits. Low inductance supply connections to the devices (one of the many advantages of SMDs) and high capacitance distributed across the board reduces the problem.

Decoupling

Decoupling capacitors provide current to devices until a power supply can respond. High frequency switching, composing a broad spectrum of current frequencies, requires several low to high frequency capacitors. This requirement is because a single capacitor typically cannot provide such a broad frequency.

A chip capacitor should be located as close as possible to a device's supply pins. To reduce series inductance the capacitor lands should be connected to the power pins using a trace width of at least 20 mil. To prevent common-mode noise, keep the trace as short as possible and do not connect directly to the plane via a thermal relief.

Tantalum capacitors (e.g. 10 uF) should be spaced evenly across the board, generally, one for every six or so ICs. These tantalum's provide current for the low frequency component of the switching transient.

Mixed Signals and Split Planes

When both analogue and digital devices are used on the same PCB, partitioning the ground plane is usually necessary. The components should be positioned so that all the devices are grouped in such a way that no digital signals will cross over the analog ground and no analog signals will cross over the digital ground.

Split or isolated planes can be used to effectively force the current associated with a particular circuit into a specific area that can be decoupled or grounded. The split plane confines high frequency currents and return paths so they can not flow across or through adjacent low frequency circuits, preventing crosstalk.

Shielding and Large Components

Large PQFP's typically require installation in a shielded equipment enclosure for compliance. However, the same piece of silicon housed in a PGA or BGA package may achieve compliance. The PGA and BGA packages have an efficient heatsink on the top of the package, which not only serves to dissipate the heat, but also acts as an EMI shield.

Routing

Orthogonal trace corners should be avoided. The debate rages, but as frequencies and edge rates continue to rise, ninety degree corners introduce excess capacitance and cause a small change in characteristic impedance. This becomes disastrous at high frequencies (e.g. 100 MHz) when electrons virtually fly off the sharp corners of the bend. Forty-five degree turns, with a minimum segment length of twice the trace width, are better. Arced corners, with the inside radius of at least the trace width, are by far the best approach for high-speed signals.

Conclusion

The competitive necessity to take maximum advantage of circuit speed and density has forced designers to pay more attention to the problems associated with transmission line effects on PCB's. In order to accurately predict potential problem areas, minimise electromagnetic interference and susceptibility and verify their design, today's PCB designers not only need to plan for EMC but also must use software to analyse the physical layout. As clock speeds approach 50 MHz, signal integrity issues should be considered.

About the Author:

Barry Olney is the Managing Director of In-Circuit Design Pty Ltd. (Melbourne, Victoria, Australia), a VeriBest Solutions Centre and CAD Services Bureau. In-Circuit Design specialise in the PCB design of high speed digital circuits and is the recipient of the Institute of Engineers, Australia 1995 Engineering Excellence Award for the MxP Sparc 20. Barry is also a lecturer in Advanced Design for Surface Mount Technology at the Australian Electronics Development Centre. For further information please contact In-Circuit Design on 03 9205 9595.