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# How to Handle the Dreaded Danglers, Part 2

**by Barry Olney**
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In Part 1 of this series, I deliberated on how dangling via stubs distort signals passing through an interconnect and also decrease the usable bandwidth of the signal. This is due to the via stub acting as a transmission line antenna, which has a resonant frequency determined by the quarter wavelength of the structure. The conventional solution to this problem is to back-drill (or control depth drill) the vias to bore out the via stub barrels, so that the via stubs are reduced in length if not completely removed. This month I will look into all the possible solutions to alleviate this issue.

### 1. Back-drill the Stub

Back-drilling is a process to remove the stub portion of a plated through-hole (PTH) via. It is a post-fabrication drilling process where the back-drilled hole is of larger diameter than the original PTH. This technology is often used instead of blind via technology to remove the stubs of connector vias in very thick high-speed backplane designs. State-of-the-art board fabrication shops are able to back-drill to within 8 mils of the signal layer, so there will always be a small stub portion attached to the via.

High-speed, SERDES, serial link-based backplanes generally have thick substrates. This is due to the system architecture and backplane to card interconnect requirements such as press-fit connectors. Back-drilling the via stub is a common practice, on thick PCBs, to minimize stub length for bit-rates greater than 3Gbps (1.5GHz). However, at transmission rates >10Gbps (5GHz), back-drilling alone may not be adequate to reduce jitter and bit error rate (BER).

Figure 1 shows the effects of excessively long via stubs on a high-speed differential pair. On the left, the differential pair is simulated using a pseudo random bit stream (PRBS) with lossy transmission lines enabled; note the open eye pattern. However, on the right, I had included via modelling, which enables the via parasitics and highlights the effects of via resonance. The high-frequency harmonics are attenuated, rolling off the signal rise time,

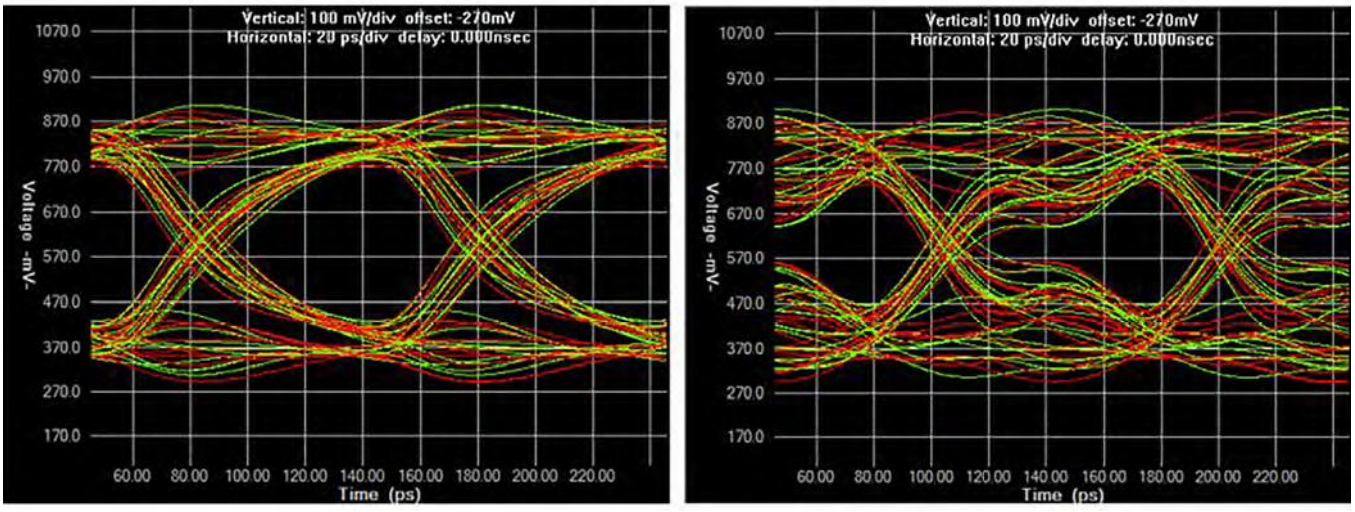


Figure 1: High-speed differential signal with via resonance (simulated in HyperLynx).

distorting the signal, reducing bandwidth and closing the eye.

Vias can appear as capacitive and/or inductive discontinuities. These parasitics contribute to the degradation of the signal as it passes through the via. At high frequencies and with thick backplane substrates, it is imperative that these issues are addressed.

Back-drilling typically requires specialized equipment, and further requires that the back-drill be precisely located over the vias. As such, the back-drilling process, especially two sided back-drilling, is expensive due to drill breakage and yield issues and is very time-consuming.

**2. Blind and Buried Vias**

Blind vias connect the outer microstrip layers to one or more inner stripline layers and may have a central reference plane between the signal layers providing a very low inductance return path. The holes are laser drilled and are typically 3-4 mils diameter. Blind vias behave like a lumped capacitor with very little inductance. And because the microvia hole is very small, it has less capacitance than a standard PTH via.

On the other hand, buried vias are used to make connections between the inner stripline layers only and may have short stubs. They have more capacitance than a standard PTH, being typically 8 mils diameter, but may still have a short stub that cannot be back-drilled from top or bottom. They may not be appropriate for high frequency design.

**3. Remove Non-Functional Pads**

Non-functional pads are pads on internal layers that are not connected to any signal or plane on that layer as illustrated in Figure 2. There is an ongoing debate regarding the influence of non-functional pads on PCB reliability, especially as related to barrel fatigue on PTH vias with high aspect ratios. The primary reason is to improve the fabricators' processes and yields as it helps manage Z-axis expansion of the board due to coefficient of thermal expansion (CTE) stresses. There is also the possibility of a short-circuit, to a plane, due to a gap in the prepreg fill, when no pad is present. However, removing non-functional via pads reduces via capacitance

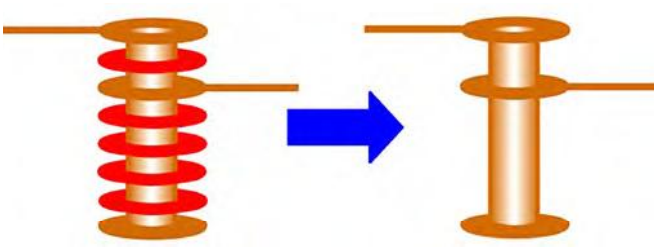

Figure 2: Non-functional via pads are removed on the right.

by approximately half, which in turn, increases impedance. So from a signal integrity point of view, this is a positive. But, check with your preferred fabricator before implementing this.

**4. Increase the Antipad Diameter**

If you follow the IPC standards, then an antipad should be 20 mils larger that the via pad diameter. However, this is not always possible (in fact very rare) in a densely packed multiplayer PCB using fine pitch BGAs. For an 8 mil via hole, the pad is typically 16 mil with an antipad of 26 mil. This allows a 9mil clearance around the pad, resulting in high plane to via capacitance. Increasing the size of the antipad, also reduces capacitance but at the same time, may well make Swiss cheese out of the reference plane. This increases the DC drop and reduces the amount of instantaneous current available to simultaneous switching devices, which is highly detrimental from a power integrity perspective.

Another alternative, that may not be very practical, is to back off the clearance to the plane, on the stub section of the via, reducing capacitance. However, this would have to be implemented manually in the PCB tool and would leave the planes, in the stub section, with wide holes reducing the effect of a solid reference plane.

So if increasing the size of the antipad is not advisable, then creating an oblong antipad may be a compromise. An oblong antipad still reduces the parasitic capacitance significantly. But at the same time, it allows the return current to flow directly between the vias to reduce loop inductance and preserve the continuity of the reference plane. Most PCB design tools will

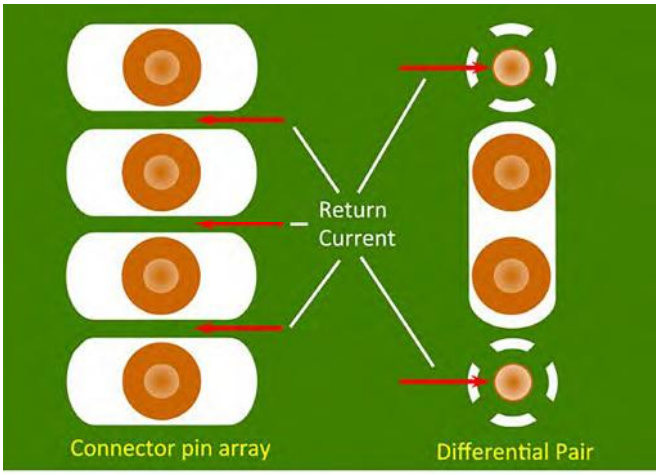


Figure 3: Oblong antipads reduce via capacitance.

allow the definition of an oblong antipad on internal layers.

Where differential pairs are present, an oblong antipad can be placed around both pairs (see Figure 3) to reduce the via-to-plane capacitance. A ground stitching via should be positioned at either end of the oblong antipad to reduce return path inductance. With connector pin arrays, the oblong clearances also preserve the continuity of the current return path in the reference plane.

### 5. Terminate the Stub

The via stub acts like an unterminated transmission line. If a terminating element is placed at the bottom end of the stub, then the reflection of the stub may be minimized. The impedance terminating element may include one or more resistors, capacitors, and/or inductors between the via stub and a ground layer. Simulation would determine the most appropriate solution. The impedance terminating element may be formed internally to the PCB, or mounted to the PCB surface. For instance, a resistor equal to the characteristic impedance of the via (50 ohms) could be placed from a single ended signal to ground or power or a 100 ohm terminating resistor across a differential pair.

### 6. Lower the Surrounding Dielectric Constant

Lowering the dielectric constant, of the material surrounding a via, by positioning non-PTHs in proximity to the interconnect is a solution proposed by Bhyrav Mutnury and colleagues, IBM Corporation. Air in the non-PTH has a dielectric constant of 1, whereas FR-4 is approximately 4. This serves to increase the resonant frequency of the via stubs. By increasing the resonant frequency of the via stub, beyond the frequency of the signal, the attenuating effects of the via stub are no longer problematic. But, it may also make Swiss cheese of the reference plane, which is not a good approach for high-speed design.

### 7. Plate the via Barrel with Lossy Material

Stuart Allen Berke and colleagues, Dell Products, have postulated reducing the Quality (Q) factor of the via stub. The resonance of a via stub can be dampened by plating the via barrel with a material having a low conductivity. For example, a via can be plated with tin, which has a conductivity of approximately 8×10^-6 S/m, while copper has a conductivity of approximately 6×10^-7 S/m. Thus, tin can be referred to as a "lossy" medium as compared to copper. Plating a via barrel with a lower conductivity material, such as tin, reduces the Q factor of the via. Resistance is inversely proportional to the conductivity of the material used to plate the via, thus a lower conductivity material results in a lower Q factor for the via dampening the resonance.

In conclusion, dangling via stubs distort a high-frequency signal and also decrease the usable bandwidth of the signal. Since the via capacitance varies in proportion to the overall size of the hole and the plane clearance of the antipads, vias should be kept small with large clearances where possible. Oblong antipads also reduce capacitance and preserve the continuity of the reference plane. Of the seven solutions put forward to alleviate this problem, using blind vias and back-drill stubs on backplanes combined with oblong antipads are the best, and most economic solutions for high-speed design.

### Points to Remember

- Back-drilling typically requires specialized equipment and is expensive.

• Blind vias behave like a lumped capacitor with very little inductance. And because the microvia hole is very small, it has less capacitance than a standard PTH via.

• Removing non-functional via pads reduces via capacitance which in turn increases impedance.

• Increasing the size of the antipad reduces capacitance but, at the same time, may well make Swiss cheese out of the reference plane increasing the DC drop and reducing the amount of instantaneous current available.

• An oblong antipad still reduces the parasitic capacitance significantly, but at the same time allows the return current to flow directly between the vias to reduce loop inductance and preserve the continuity of the reference plane.

• A terminating element placed at the bottom end of the stub reduces signal reflection.

• Lowering the dielectric constant, of the surround material, and tin plating the via barrel are possible but may not be practical solutions.

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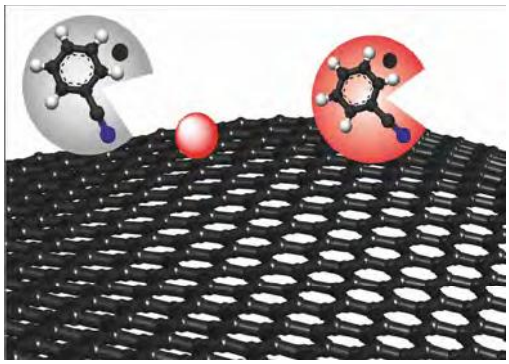
# Low-cost and Defect-free Graphene



Chemists at Friedrich-Alexander-Universiät Erlangen-Nürnberg (FAU) have now succeeded in producing defect-free graphene directly from graphite for the first time.

Graphene is two-dimensional and consists of a single layer of carbon atoms. It is particularly good at conducting electricity and heat, transparent and flexible yet strong. Graphene's unique properties make it suitable for use in a wide range of pioneering technologies, such as in transparent electrodes for flexible displays.

A common way of synthesising graphene is through chemical exfoliation of graphite. In this process, metal ions are embedded in graphite, which is made of carbon, resulting in what is known as an intercalation compound. The individual layers of carbon - the graphene - are separated using solvents. The stabilised graphene then has to be separated from the solvent and reoxidised. However, defects in the individual layers of carbon, such as hydration and oxidation of carbon atoms in the lattice, can occur during this process. FAU researchers have now found a solution to this problem. By adding the solvent benzonitrile, the graphene can be removed without any additional functional groups forming - and it remains defect-free.

"This discovery is a break-through for experts in the international field of reductive graphene synthesis,' Professor Hirsch explains. 'Based on this discovery we can expect to see major advancements in terms of the applications of this type of graphene which is produced using wet chemical exfoliation. An example could be cutting defect-free graphene for semi-conductor or sensor technology."