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PCB Design Techniques for DDR, DDR2 & DDR3

(Part 2)

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SUMMARY

This second and last part in a series examining PCB Design Techniques will look at the comparison of DDR2 to DDR3; DDR3 design guidelines; pre-layout analysis; critical placement; an example of design rules; and finally, the post-layout analysis.

One major difference between DDR2 and DDR3 SDRAM is the use of levelling. To improve signal integrity and support higher frequency operations, the JEDEC committee defined a fly-by termination scheme used with the clocks, command and address bus signals. Fly-by topology reduces simultaneous switching noise (SSN) by deliberately causing flight-time skew between the data and strobes at every chip/DRAM, requiring controllers to compensate for this skew by adjusting the timing per byte lane (Table 1).

During a write, DQS groups are launched at separate times to coincide with a clock.

<table>
<thead>
<tr>
<th>DDR2/DDR3 Comparison</th>
<th>DDR2</th>
<th>DDR3</th>
</tr>
</thead>
<tbody>
<tr>
<td>Max Clock Frequency</td>
<td>533/1066</td>
<td>800/1600</td>
</tr>
<tr>
<td>ODT</td>
<td>Static</td>
<td>Dynamic</td>
</tr>
<tr>
<td>VDD</td>
<td>1.8V</td>
<td>1.5V (may also be 1.35V)</td>
</tr>
<tr>
<td>VTT</td>
<td>0.9V</td>
<td>0.75V</td>
</tr>
<tr>
<td>Vref</td>
<td>0.9V</td>
<td>0.75V</td>
</tr>
<tr>
<td>Input thresholds</td>
<td>0.9V</td>
<td>0.75V</td>
</tr>
<tr>
<td>Match Addr/CMD/CTRL to CLK tightly</td>
<td>yes</td>
<td>yes</td>
</tr>
<tr>
<td>Match DQ/DMO/DSQ tightly</td>
<td>yes</td>
<td>yes</td>
</tr>
<tr>
<td>Match DQS to clock loosely</td>
<td>yes</td>
<td>not required</td>
</tr>
</tbody>
</table>

Table 1.
arriving at components on the DIMM/PCB, and must meet the timing parameter between the memory clock and DQS defined as tDQSS of ± 0.25 tCK.

The design process can be simplified using the new levelling feature of DDR3 and controller IC’s. The fly-by daisy chain topology increases the complexity of the data path and controller design to achieve levelling, but also greatly improves performance and eases board layout for DDR3.

**DDR3 Design Guidelines—**

**Critical Constraints:**

- Clock nets, DQ (data) and DQS (strokes) are routed differentially. 4.5” max length +/- 25MIL
- Net length from driver to first DIMM or chip: between 2” to 3” max depending on load
- Net length between DIMM’s or chips: 0.5”
- Net length from last DIMM or Chip to the VTT Termination: 0.2” to 0.55”
- All DSQ/DQ (data and data strobe) should be minimized to reduce the skew within groups (or lanes) and across groups. 50 MIL within groups and 800 MIL across groups.
- Skew between address nets should be 200MIL. Address and command nets are daisy chained with a VTT pull-up for termination.

Other constraints to consider:

- DDR3 data nets have dynamic On-Die Termination (ODT) built into the controller and SDRAM. The configurations are 40Ω, 60Ω and 140Ω so VTT pull-up is not necessary.
- Zo for DDR3 is 50Ω. Zdiff is 100Ω.

**Pre-layout Analysis**

I can’t emphasize enough the importance of pre-layout analysis. Without which, you are just relying on luck—which is not a design parameter. The pre-layout simulation is used to predict and eliminate signal integrity issues early, proactively constraining routing and optimizing clock, critical signal topologies and terminations prior to board layout.

As previously mentioned, the value and placement of the series resistors and VTT pull-ups for data, address and command signals depends on the distances between the loads, number of loads and the stackup of the board and are best determined by simulation. The series terminator may not be required if a single SDRAM is used and the trace length is short—but how do you know if you don’t simulate the proposed layout?

In general, try to keep the SDRAM as close as possible to the controller, but bear in mind that sometimes it will not be not possible because of other physical constraints. Also, if there are two or more SDRAM chips, this becomes more difficult and requires extended signal lengths terminators. Now the question becomes, where should they be placed and what values should be used?

The series terminator would normally be placed close to the driver. Surprisingly, however, in the above case, the signal integrity

**Figure 1:** 2.375<x<2.652” DDR3 topology using levelling.
Final Post-Layout Analysis

The final post-layout analysis includes a batch mode simulation of all the nets. This flags signal integrity, crosstalk and EMI hot spots. Basically, look carefully through this report to see any issues that may have to be dealt with.

The batch mode simulation reports:
- Signal Integrity issues including over/under shoot.
- Nets that are too long and need termination.
- Crosstalk from multiple aggressor nets.
- Possible EMI sources.

Go through these items one at a time and look at whether there needs to be action taken. For instance, a long ‘Reset’ signal or a signal going to a static pull-up may be reported as being too long, but we can obviously ignore these particular warnings. Another possible case that needs to be addressed: a critical signal that is routed over the Manhattan length and needs termination.

Crosstalk is quite common in high speed designs because of the cramped real estate; signals have to be packed tightly into a small area. Crosstalk can be minimized by increasing trace spacing and by reducing the signal layer to reference plane separation. Try to keep prepreg thickness to 3 MIL to tightly couple the signals to the plane. Also, it may be necessary to add additional planes to the stackup to isolate the offending aggressor signals. Routing adjacent signal layers orthogonally also helps reduce noise coupling.

Crosstalk problems can cause intermittent operation due to timing glitches and interference, dramatically reducing your product’s reliability. So, it is best to address these issues at the source.

If a good job has been done routing the high-speed signals, on the internal layers and away from the edges of the board, then EMI should be minimal. However, if there is an EMI
issue then different routing strategies can be tried to eliminate the problem. EMC can be measured, during the design process, to FCC, CISPR, VCCI Class A & B standard—this alone saves multiple iterations of a design.

All critical high-speed signals should be individually checked. Signal flight times need to be within spec, and eye diagrams need to have eyes wide open.

By simulating during the design process, you can be assured that your PCB layout will be of the highest quality and will pass the relevant EMC tests—saving you time, money and frustration for a fraction of the cost of board iterations and multiple compliancy testing. Plus, the simulation can be done before the design is finalized (before Gerber output or even earlier in the design process) to further reduce production time and costs.

**Table 2.**

<table>
<thead>
<tr>
<th>Rule Name</th>
<th>Rule Type</th>
<th>Scope</th>
<th>Attribute</th>
</tr>
</thead>
<tbody>
<tr>
<td>Length</td>
<td>Length</td>
<td>(InNetClass('Lane0') AND InNetClass('Lane1') AND InNetClass('Lane2'))</td>
<td>Min Length = 500mil Max Length = 1000mil</td>
</tr>
<tr>
<td>Parallel Segment</td>
<td>Parallel Segment</td>
<td>All - All</td>
<td>Gap = 4mil Limit = 500mil Layer = Same Layer</td>
</tr>
<tr>
<td>USB Data and Control</td>
<td>Matched Net Lengths</td>
<td>InNetClass('USB_length')</td>
<td>Tolerance = 100mil</td>
</tr>
<tr>
<td>Diff Pair USB Matched Lengths</td>
<td>Matched Net Lengths</td>
<td>InDifferentialPair ('USB')</td>
<td>Tolerance = 25mil</td>
</tr>
<tr>
<td>Diff Pair Matched Lengths</td>
<td>Matched Net Lengths</td>
<td>(InDifferentialPairClass ('All Differential Pairs'))</td>
<td>Tolerance = 25mil</td>
</tr>
<tr>
<td>DDR CLK Matched Lengths</td>
<td>Matched Net Lengths</td>
<td>InDifferentialPair ('DDR_MCK')</td>
<td>Tolerance = 25mil</td>
</tr>
<tr>
<td>DDR2 CTL</td>
<td>Matched Net Lengths</td>
<td>InNetClass('DDR2_CTL')</td>
<td>Tolerance = 200mil</td>
</tr>
<tr>
<td>DDR2 Addr</td>
<td>Matched Net Lengths</td>
<td>InNetClass('DDR2_Addr')</td>
<td>Tolerance = 200mil</td>
</tr>
<tr>
<td>Lane3</td>
<td>Matched Net Lengths</td>
<td>InNetClass('Lane3')</td>
<td>Tolerance = 50mil</td>
</tr>
<tr>
<td>Lane2</td>
<td>Matched Net Lengths</td>
<td>InNetClass('Lane2')</td>
<td>Tolerance = 50mil</td>
</tr>
<tr>
<td>Lane1</td>
<td>Matched Net Lengths</td>
<td>InNetClass('Lane1')</td>
<td>Tolerance = 50mil</td>
</tr>
<tr>
<td>Lane0</td>
<td>Matched Net Lengths</td>
<td>InNetClass('Lane0')</td>
<td>Tolerance = 50mil</td>
</tr>
<tr>
<td>All Lanes</td>
<td>Matched Net Lengths</td>
<td>(InNetClass('Lane0') AND InNetClass('Lane1') AND InNetClass('Lane2'))</td>
<td>Tolerance = 500mil</td>
</tr>
</tbody>
</table>

**References:**
1. Advanced Design for SMT – Barry Olney, In-Circuit Design Pty Ltd.
2. JEDEC Specifications JESD 79F, JESD79-2E & JESD79-3D.
3. Altera Board Layout Guidelines, EMI Plan Board.

Barry Olney is Managing Director of In-Circuit Design Pty Ltd (ICD), Australia, a PCB Design Service Bureau and Board Level Simulation Specialist. Among many other awards through the years, ICD was awarded “Top 2005 Asian Distributor Marketing” and “Top 2005 Worldwide Distributor Marketing” by Mentor Graphics, Board System Division.