

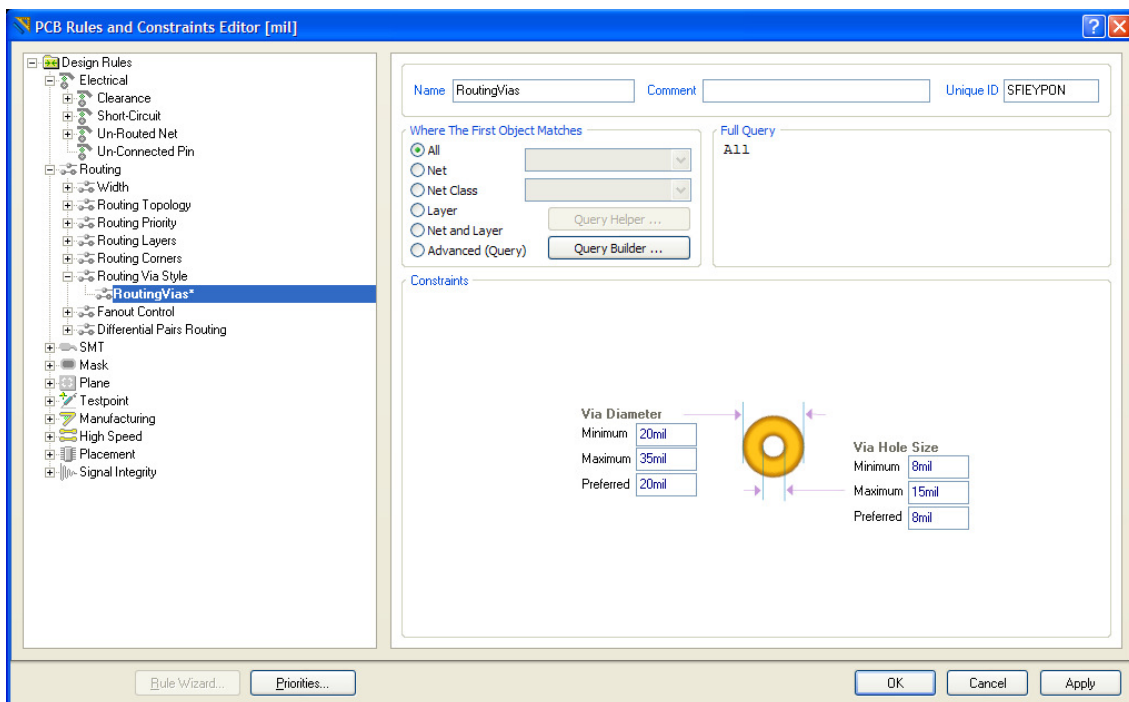
The Altium Designer Stackup Planner Bi-directional Interface imports the substrate configuration from the ICD Stackup Planner and automatically creates the corresponding Layers in Altium Designer configuring the Layer Stack Manager. Also, Design Rules for Trace Width, Clearance and Differential Pairs are automatically created in Altium Designer enabling the user to route each layer and differential pair to the calculated single ended or differential impedance.

The interface can also export the Altium Designer Layers from the Layer Stack Manager and Trace Width/Clearances into the ICD Stackup Planner for the calculation of impedance and trace current. The stackup can then be modified to obtain the desired impedances and imported back into Altium Designer.

The Altium Designer Stackup Planner Bi-directional Interface was jointly developed by DesktopEDA and In-Circuit Design. The interface currently supports Altium Designer S09.

Please Note: Before importing the Stackup into Altium Designer the via size should be set as this impacts on the maximum gap for differential pairs.

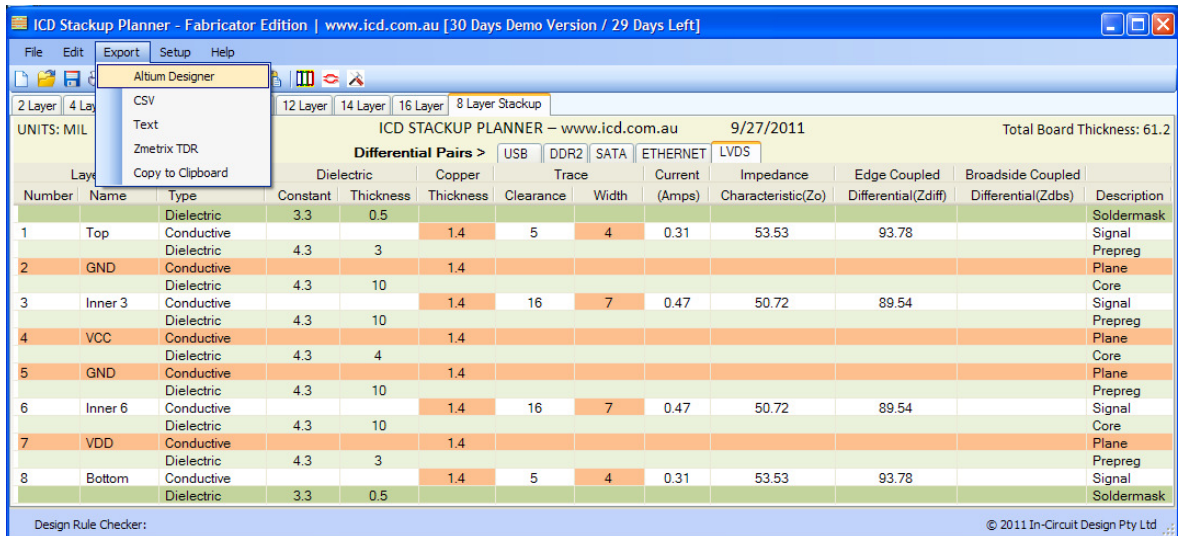
In Altium Designer open Design -> Rules -> Routing -> RoutingVias and set the via and hole diameters to the desired values.



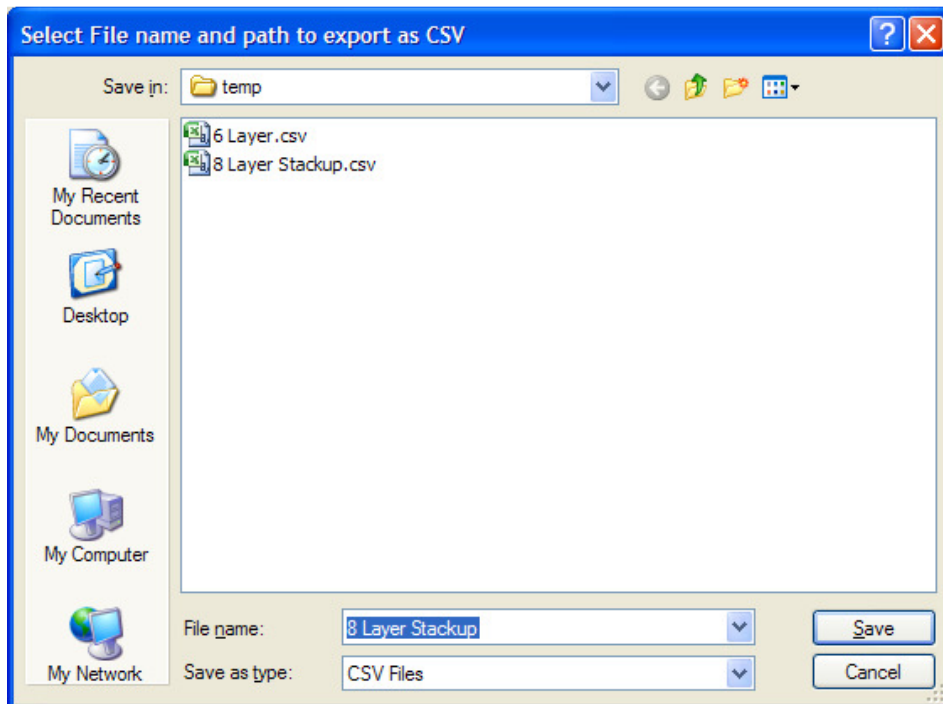
Import a Substrate from the ICD Stackup Planner into Altium Designer:

1. Open the ICD Stackup Planner and create the required stackup from the available default stackups or create your own from scratch. Adjust the variables to achieve the desired single ended and differential impedances of each layer.
2. Only one differential pair can be exported to Altium Designer. In the Stackup Planner highlight Differential Pair TAB to be exported.

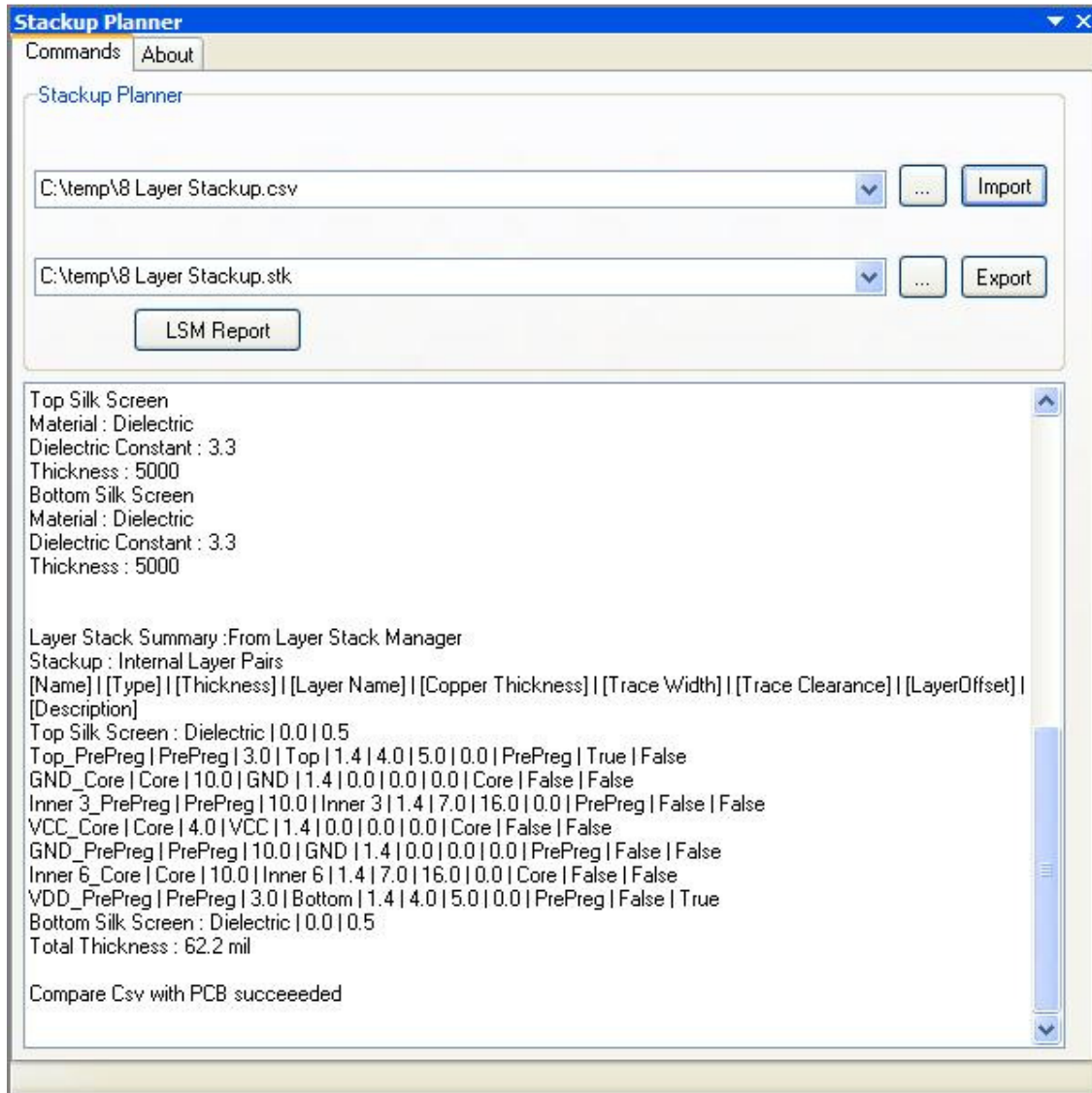
3. Select Export -> Altium Designer



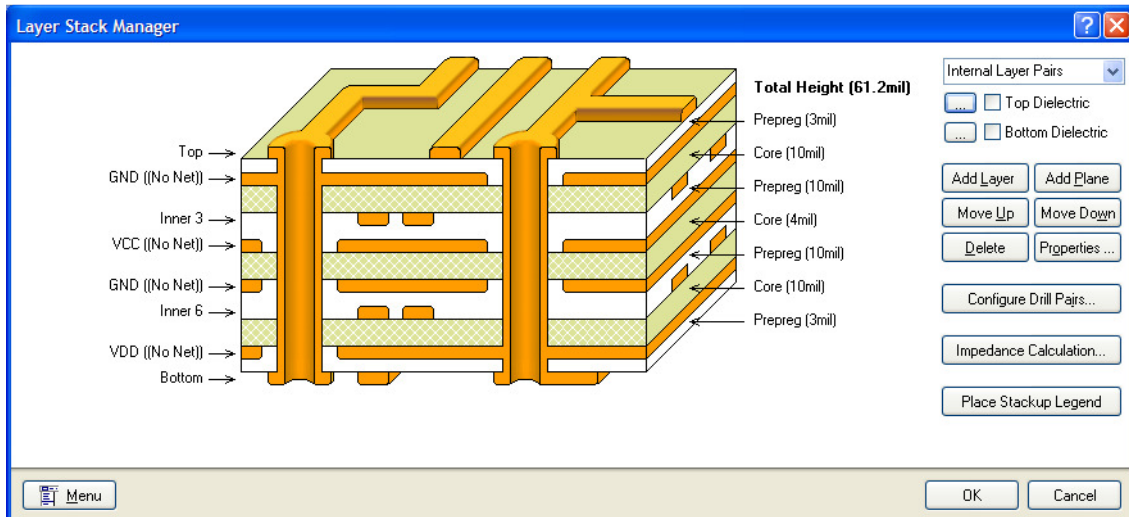
4. Fill in the file name with a .CSV extension to export.



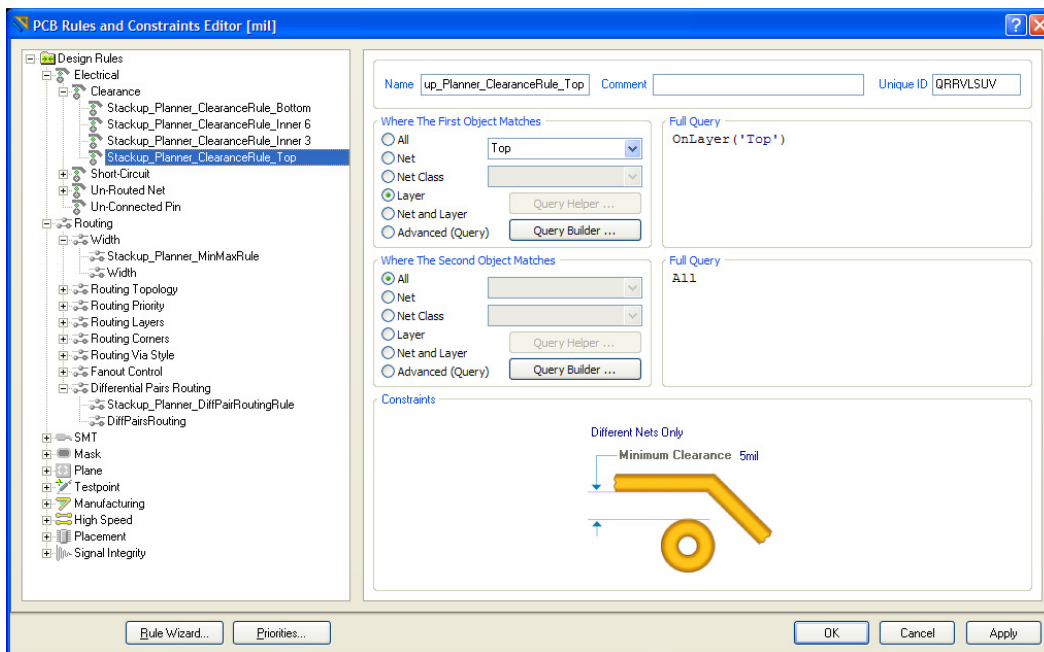
5. Open Altium Designer and go to PCB -> Stackup Planner



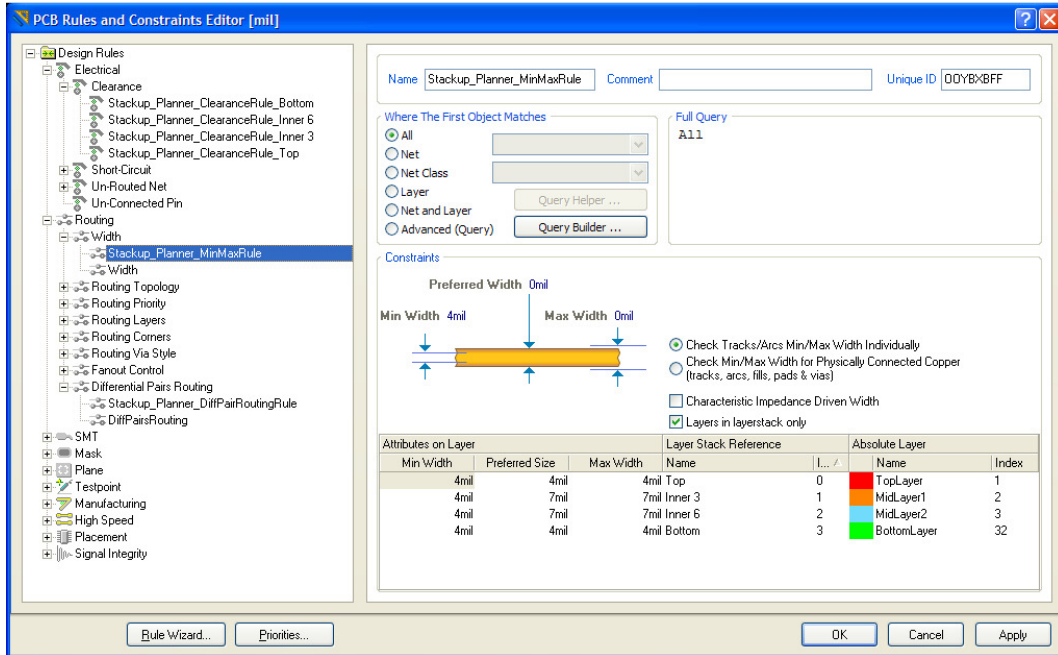
6. Browse to find the CSV created in step 4)
7. Click 'Import' to bring the substrate into Altium Designer
8. Open Design -> Layer Stack Manager to see the new substrate configuration



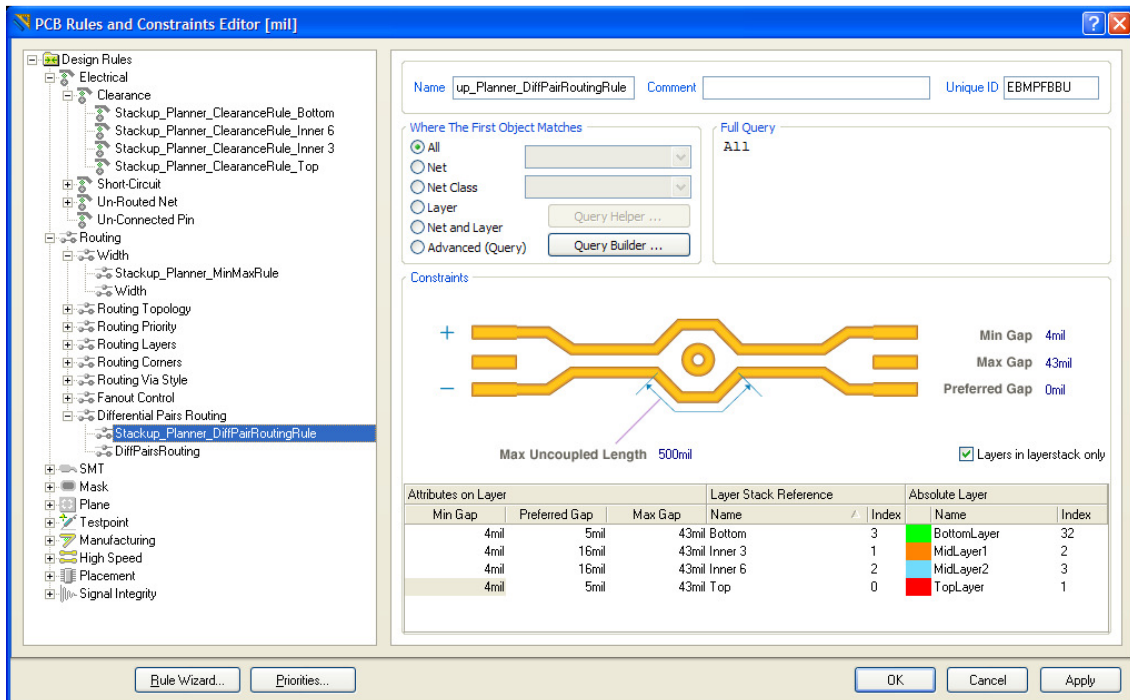
9. Open Design -> Rules and you will note that a number of new entries have been imported. The new rules all have the prefix Stackup_Planner
 - a. Stackup_Planner_ClearanceRule_Top
 - b. Stackup_Planner_ClearanceRule_Inner 3
 - c. Stackup_Planner_ClearanceRule_Inner 6
 - d. Stackup_Planner_ClearanceRule_Bottom
 - e. Stackup_Planner_MinMaxRule
 - f. Stackup_Planner_DiffPairRoutingRule



a – d. The clearance rules are set to the Stackup Planner clearance for each layer. The number of clearance rules depends on the number of signal layers in the original stackup.

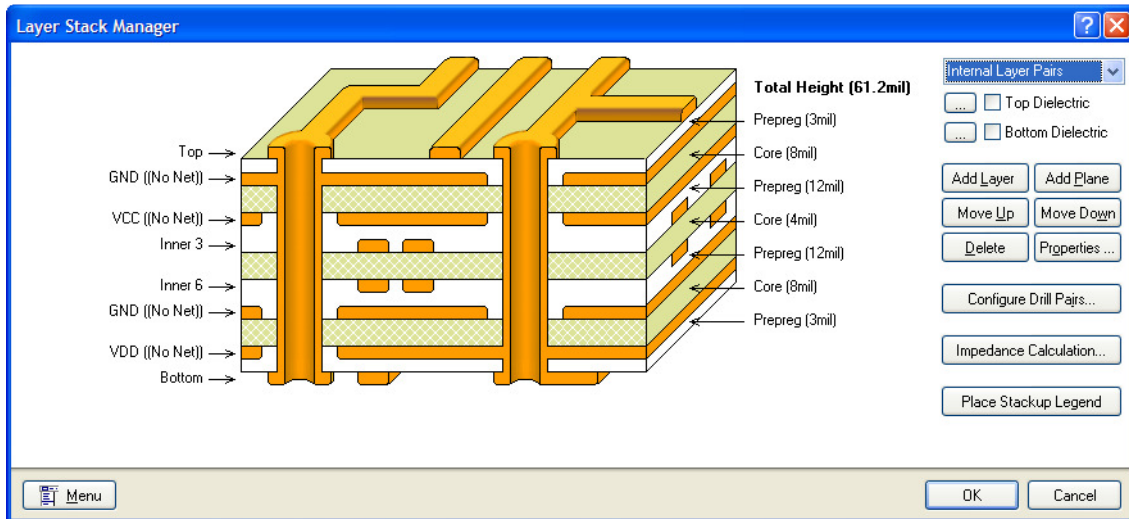


- e. The Stackup_Planner_MinMaxRule has each layer set to the preferred size defined in the Stackup Planner. Min width is 4 MIL, Max is the same as the preferred.

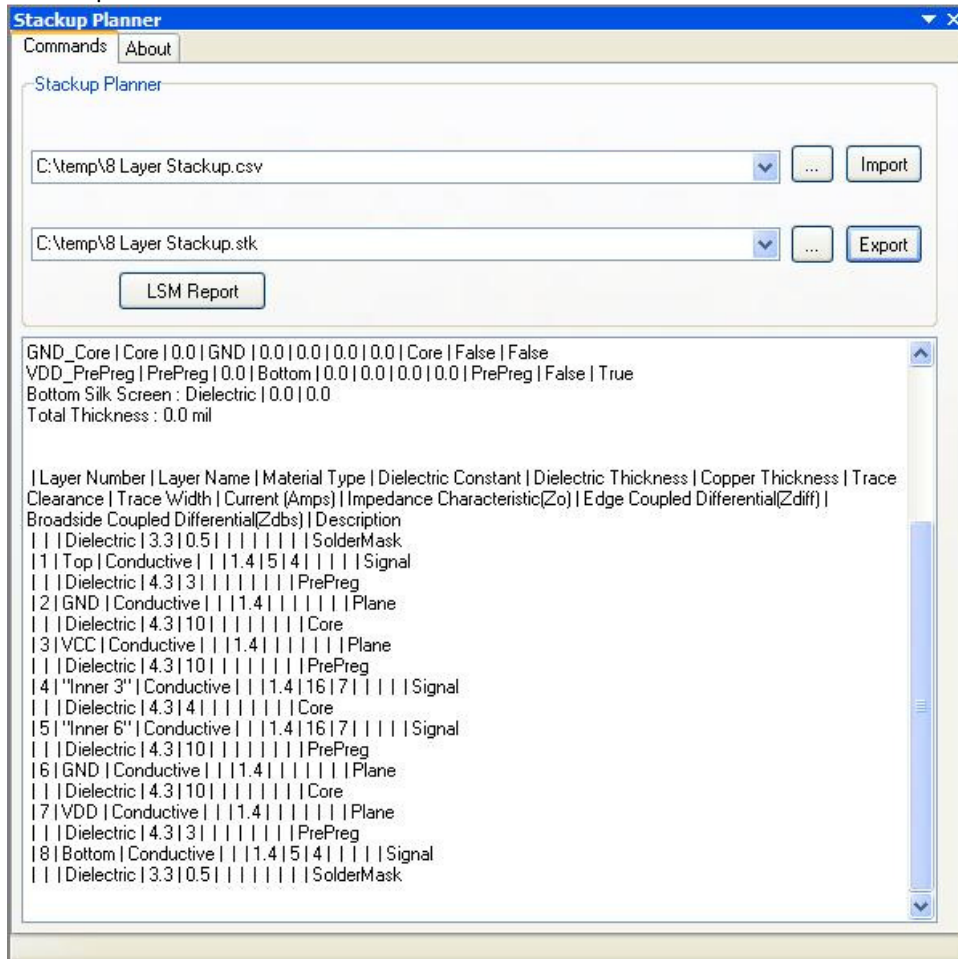


- f. The Stackup_Planner_DiffPairRoutingRule has the preferred gap of the differential pairs set to the clearance for each layer as defined in the Stackup Planner. Min Gap is 4 MIL, Max is the maximum via size as set in the first step plus twice the minimum clearance. $35 + 8 = 43$ MIL. This allows the differential pairs to separate around an obstacle (via).

Export a Substrate from Altium Designer into the ICD Stackup Planner:



1. Adjust the stackup in Altium Designer to the desired configuration.
2. In Altium Designer go to PCB -> Stackup Planner
3. Select the file name (.stk) to export to the stackup planner
4. Click Export



- In the ICD Stackup Planner, go to File -> Open (the .stk created in step 3). The impedances will be automatically calculated when the file is loaded into the Stackup Planner.

UNITS: MIL ICD STACKUP PLANNER – www.icd.com.au 9/28/2011 Total Board Thickness: 61.2

Differential Pairs > Pair 1

Layer	Material		Dielectric		Copper	Trace		Current	Impedance	Edge Coupled	Broadside Coupled	Description
Number	Name	Type	Constant	Thickness	Thickness	Clearance	Width	(Amps)	Characteristic(Zo)	Differential(Zdiff)	Differential(Zdbs)	
1	Top	Conductive	3.3	0.5	1.4	5	4	0.31	53.53	93.78		SolderMask
		Dielectric	4.3	3								Signal
2	GND	Conductive	4.3	8	1.4							Plane
		Dielectric	4.3	12								Core
3	VCC	Conductive	4.3	8	1.4							Plane
		Dielectric	4.3	12								PrePreg
4	"Inner 3"	Conductive	4.3	4	1.4	16	7	0.47	60.43	113.17	38.97	Signal
		Dielectric	4.3	4								Core
5	"Inner 6"	Conductive	4.3	4	1.4	16	7	0.47	60.43	113.17	38.97	Signal
		Dielectric	4.3	12								PrePreg
6	GND	Conductive	4.3	8	1.4							Plane
		Dielectric	4.3	8								Core
7	VDD	Conductive	4.3	3	1.4							Plane
		Dielectric	4.3	3								PrePreg
8	Bottom	Conductive	3.3	0.5	1.4	5	4	0.31	53.53	93.78		Signal
		Dielectric	3.3	0.5								SolderMask

The LSM Report lists the current configuration of the Layer Stack Manager in Altium Designer.

The Rules Report summarizes the Trace Width and Clearance for each layer of the stackup and specifies whether the units are metric or imperial.

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